	L #	Hits	Search Text	DBs
1	L1	360962	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item)	USPAT; US-PGPUB
2	L2	360976	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item suboperand consituent)	USPAT; US-PGPUB
3	L3	271330	(portion part set subset) near20 (operand pack$2 composite compound)	USPAT; US-PGPUB
4	L4	1556	2 near30 3	USPAT; US-PGPUB
5	L5	325714	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near10 (element item suboperand consituent)	USPAT; US-PGPUB
6	L6	237043	(portion part set subset) near10 (operand pack$2 composite compound)	USPAT; US-PGPUB
7	L7	875	5 near20 6	USPAT; US-PGPUB
8	L11	150	7 and (operand data).ab,ti.	USPAT; US-PGPUB
9	L12	57	4 and (operand data).ab,ti. not 11	USPAT; US-PGPUB
10	L13	226532	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item suboperand consituent)	EPO; JPO; DERWENT; IBM_TDB
11	L14	115651	(portion part set subset) near20 (operand pack$2 composite compound)	EPO; JPO; DERWENT; IBM_TDB
12	L15	575	13 near30 14	EPO; JPO; DERWENT; IBM_TDB
13	L16	49	15 and (operand data).ab,ti.	EPO; JPO; DERWENT; IBM_TDB

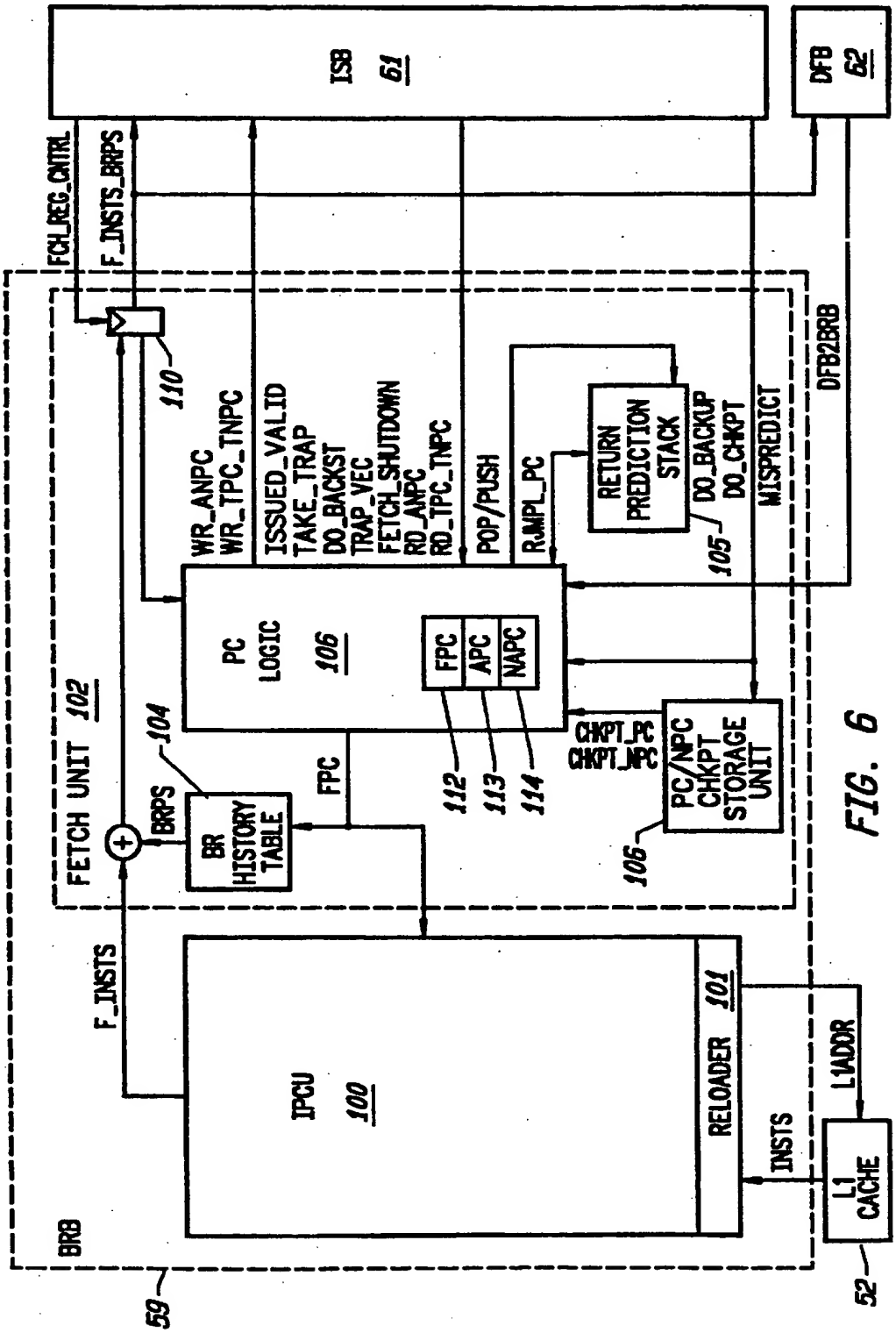

ISB 61
DFB 62
FCH_REG_CNTRL
F_INSTS_BRPS
110
WR_ANPC
WR_TPC_TNPC
ISSUED_VALID
TAKE_TRAP
DO_BACKST
TRAP_VEC
FETCH_SHUTDOWN
RD_ANPC
RD_TPC_TNPC
POP/PUSH
RJMPL_PC
RETURN PREDICTION STACK
105
DO_BACKUP
DO_CHKPT
MISPREDICT
DFB2BRB
PC LOGIC 106
FPC
APC
NAPC
112
113
114
CHKPT_PC
CHKPT_NPC
PC/NPC CHKPT STORAGE UNIT
106
FETCH UNIT 102
104
BRPS
BR HISTORY TABLE
FPC
F_INSTS
IPCU 100
RELOADER 101
L1ADDR
INSTS
L1 CACHE
52
BRB
59

FIG. 6

	Document ID	U	Title	Current OR
1	US 20030 20041 9 A1	☐	Non-copy shared stack and register file device and dual language processor structure using the same	712/202
2	US 20030 19352 5 A1	☒	Expedited selection of items from a list within a drop down menu of an eye diagram analyzer	345/810
3	US 20030 18530 9 A1	☒	Method and system in a transceiver for controlling a multiple-input, multiple-output communications channel	375/257
4	US 20030 17710 5 A1	☒	Gene expression programming algorithm	706/13
5	US 20030 15440 0 A1	☒	Method and network element for providing secure access to a packet data network	713/201
6	US 20030 15207 6 A1	☒	Vertical instruction and data processing in a network processor architecture	370/389
7	US 20030 13121 9 A1	☒	Method and apparatus for unpacking packed data	712/225
8	US 20030 08089 1 A1	☒	Resistance changeable device for data transmission system	341/155
9	US 20030 06545 9 A1	☒	Expandable intelligent electronic device	702/62
10	US 20030 02075 7 A1	☒	DISPLAY CONTROL APPARATUS AND DISPLAY CONTROL SYSTEM FOR SWITCHING CONTROL OF TWO POSITION IDICATION MARKS	345/790
11	US 20030 01670 3 A1	☒	Method, device and software for digital inverse multiplexing	370/535
12	US 20020 19674 8 A1	☒	Radio link and method for operating it	370/310
13	US 20020 17820 0 A1	☒	Circuit for selectively providing maximum or minimum of a pair of floating point operands	708/495
14	US 20020 15699 7 A1	☒	Method for mapping instructions using a set of valid and invalid logical to physical register assignments indicated by bits of a valid vector together with a logical register list	712/217
15	US 20020 12410 4 A1	☒	Network element and a method for preventing a disorder of a sequence of data packets traversing the network	709/238
16	US 20020 12222 8 A1	☒	Network and method for propagating data packets across a network	398/98
17	US 20020 12222 5 A1	☒	Multiport wavelength division multiplex network element	398/34

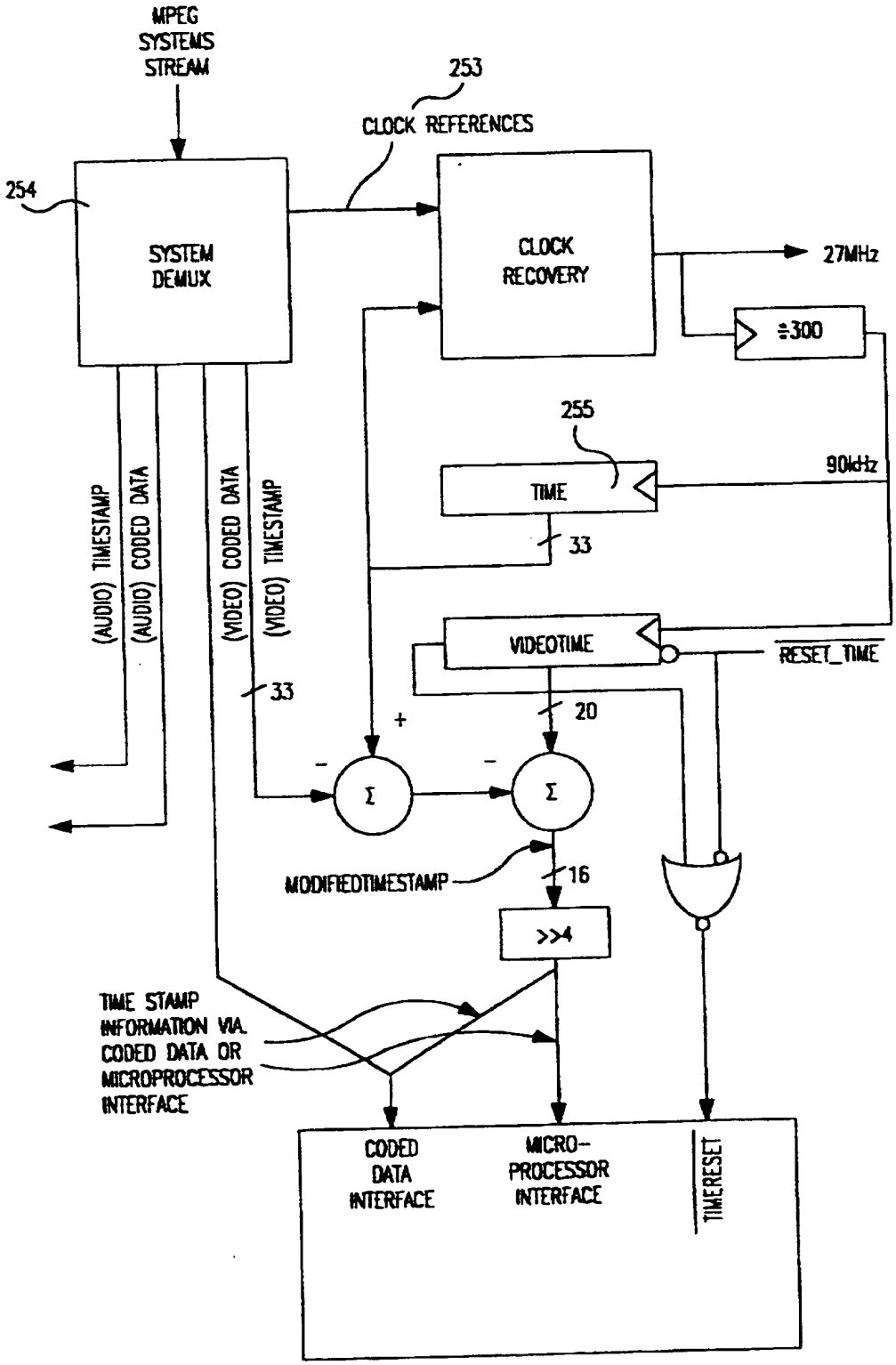

MPEG SYSTEMS STREAM
253
CLOCK REFERENCES
254
SYSTEM DEMUX
CLOCK RECOVERY
27MHz
÷300
255
TIME
90kHz
33
(AUDIO) TIMESTAMP
(AUDIO) CODED DATA
(VIDEO) CODED DATA
(VIDEO) TIMESTAMP
VIDEOTIME
RESET_TIME
33
20
+
−
−
Σ
Σ
MODIFIEDTIMESTAMP
16
>>4
TIME STAMP INFORMATION VIA CODED DATA OR MICROPROCESSOR INTERFACE
CODED DATA INTERFACE
MICRO-PROCESSOR INTERFACE
TIMERESET

FIG. 122

	Document ID	U	Title	Current OR
18	US 20020 11214 7 A1	☒	Shuffle instructions	712/223
19	US 20020 11198 7 A1	☒	Data exchange system comprising portable data processing units	709/201
20	US 20020 09770 0 A1	☒	Apparatus, and associated method, for utilizing antenna information determinative of antenna operation in a wireless mesh network	370/338
21	US 20020 09478 0 A1	☒	Method and apparatus for signaling among a plurality of agents	455/41.2
22	US 20020 08770 9 A1	☒	Stream processing node	709/231
23	US 20020 08557 4 A1	☒	Stream switch fabric	370/412
24	US 20020 06934 6 A1	☒	METHOD FOR MAPPING INSTRUCTIONS USING A SET OF VALID AND INVALID LOGICAL TO PHYSICAL REGISTER ASSIGNMENTS INDICATED BY BITS OF A VALID VECTOR TOGETHER WITH A LOGICAL REGISTER LIST	712/216
25	US 20020 06773 1 A1	☒	Dynamic data tunnelling	370/401
26	US 20020 06601 3 A1	☒	Maintaining end-to-end synchronization on a telecommunications connection	713/151
27	US 20020 06364 1 A1	☒	Dual mode data compression for operating code	341/87
28	US 20020 06233 1 A1	☒	A METHOD AND APPARATUS FOR COMPUTING A PACKED SUM OF ABSOLUTE DIFFERENCES	708/524
29	US 20020 06099 1 A1	☒	Method and apparatus for improving the transmission quality in a packet-oriented data transmission network	370/286
30	US 20010 05401 5 A1	☒	Method for facilitating the exchange of information over a computer network	705/26
31	US 20010 05315 0 A1	☒	Packet processor with programmable application logic	370/392
32	US 20010 04205 8 A1	☒	APPARATUS AND METHOD FOR MANAGING MEMORY USE BY SOFTWARE OBJECTS	707/1
33	US 20010 01864 6 A1	☒	USB simulation apparatus and storage medium	703/13
34	US 66282 23 B2	☒	Resistance changeable device for data transmission system	341/155
35	US 65742 44 B1	☒	Determining time stamps in a data acquisition system	370/503

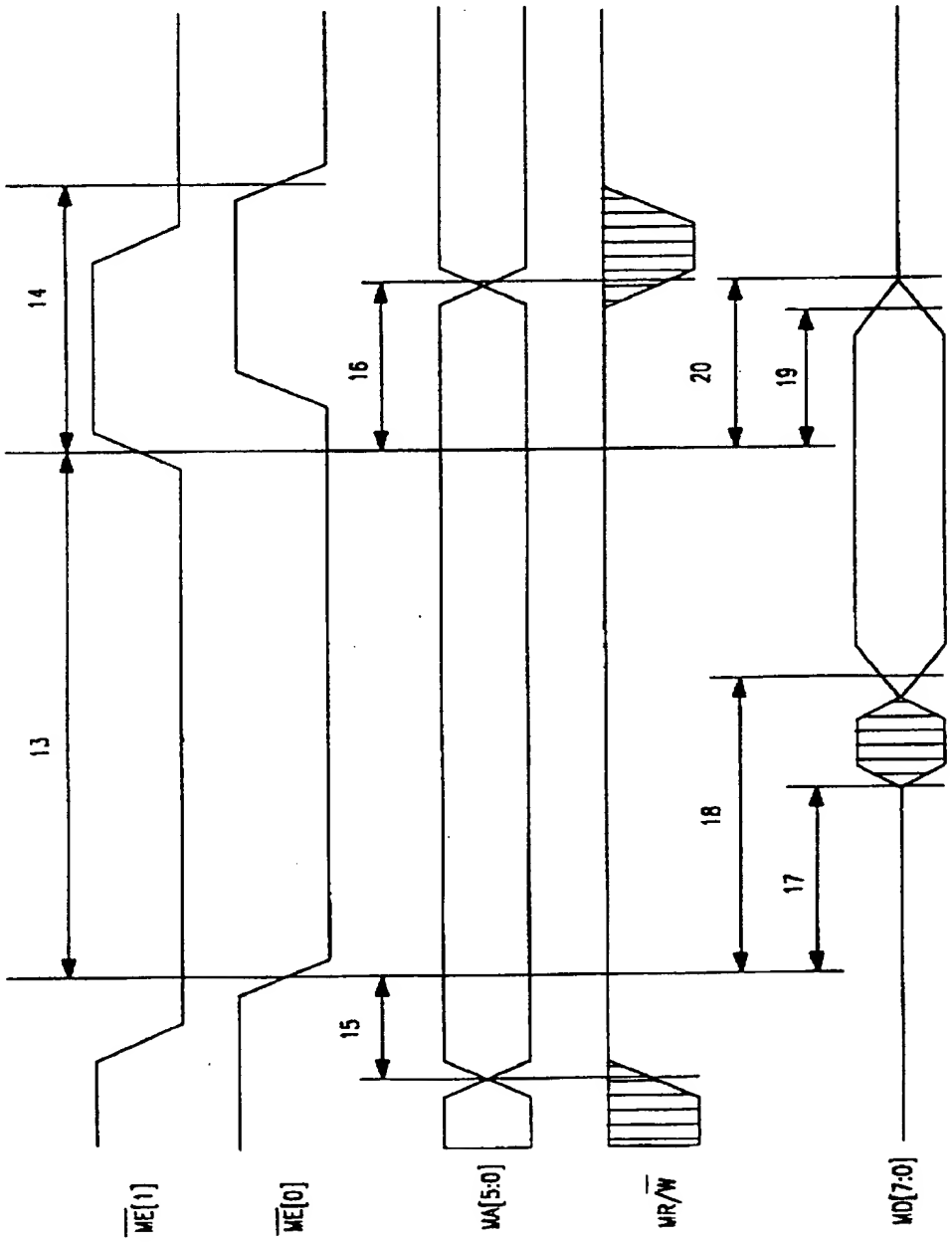

14
13
16
15
20
19
18
17
$\overline{WE}[1]$
$\overline{WE}[0]$
WA[5:0]
$\overline{WR}/W$
WD[7:0]

FIG. 123

	Document ID	U	Title	Current OR
36	US 6553005 B1	☒	Method and apparatus for load apportionment among physical interfaces in data routers	370/285
37	US 6545720 B1	☒	Method for the display of teletext headers	348/468
38	US 6538675 B2	☒	Display control apparatus and display control system for switching control of two position indication marks	345/856
39	US 6516406 B1	☒	Processor executing unpack instruction to interleave data elements from two packed data	712/225
40	US 6477185 B1	☒	Demultiplexing and decoding apparatus for coded audio and video data	370/536
41	US 6438676 B1	☒	Distance controlled concatenation of selected portions of elements of packed data	712/22
42	US 6411227 B1	☒	Dual mode data compression for operating code	341/65
43	US 6405304 B1	☒	Method for mapping instructions using a set of valid and invalid logical to physical register assignments indicated by bits of a valid vector together with a logical register list	712/216
44	US 6385645 B1	☒	Data exchange system comprising portable data processing units	709/208
45	US 6377970 B1	☒	Method and apparatus for computing a sum of packed data elements using SIMD multiply circuitry	708/603
46	US 6366732 B1	☒	Machine readable recording medium, reproduction apparatus, and method for setting pre-reproduction parameters and post-reproduction parameters for video objects	386/95
47	US 6356707 B1	☒	Multimedia optical disk, reproduction apparatus and method for achieving variable scene development based on interactive control	386/95
48	US 6326967 B1	☒	Image creating apparatus, image creating method, and computer-readable recording medium containing image creating program	345/427
49	US 6311280 B1	☒	Low-power memory system with incorporated vector processing	713/320
50	US 6295597 B1	☒	Apparatus and method for improved vector processing to support extended-length integer arithmetic	712/8
51	US 6288723 B1	☒	Method and apparatus for converting data format to a graphics card	345/644
52	US 6281861 B1	☒	Spatial light modulator and directional display	345/32
53	US 6256634 B1	☒	Method and system for purging tombstones for deleted data items in a replicated database	707/100
54	US 6243803 B1	☒	Method and apparatus for computing a packed absolute differences with plurality of sign bits using SIMD add circuitry	712/210
55	US 6236410 B1	☒	Efficient methods for the evaluation of a graphical programming language	345/440
56	US 6226446 B1	☒	Machine readable recording medium, reproduction apparatus and method for controlling selection of menu items within a video object	386/95
57	US 6185365 B1	☒	Multimedia optical disk, reproduction apparatus and method for achieving variable scene development based on interactive control	386/95
58	US 6148427 A	☒	Method and apparatus for test data generation	714/738

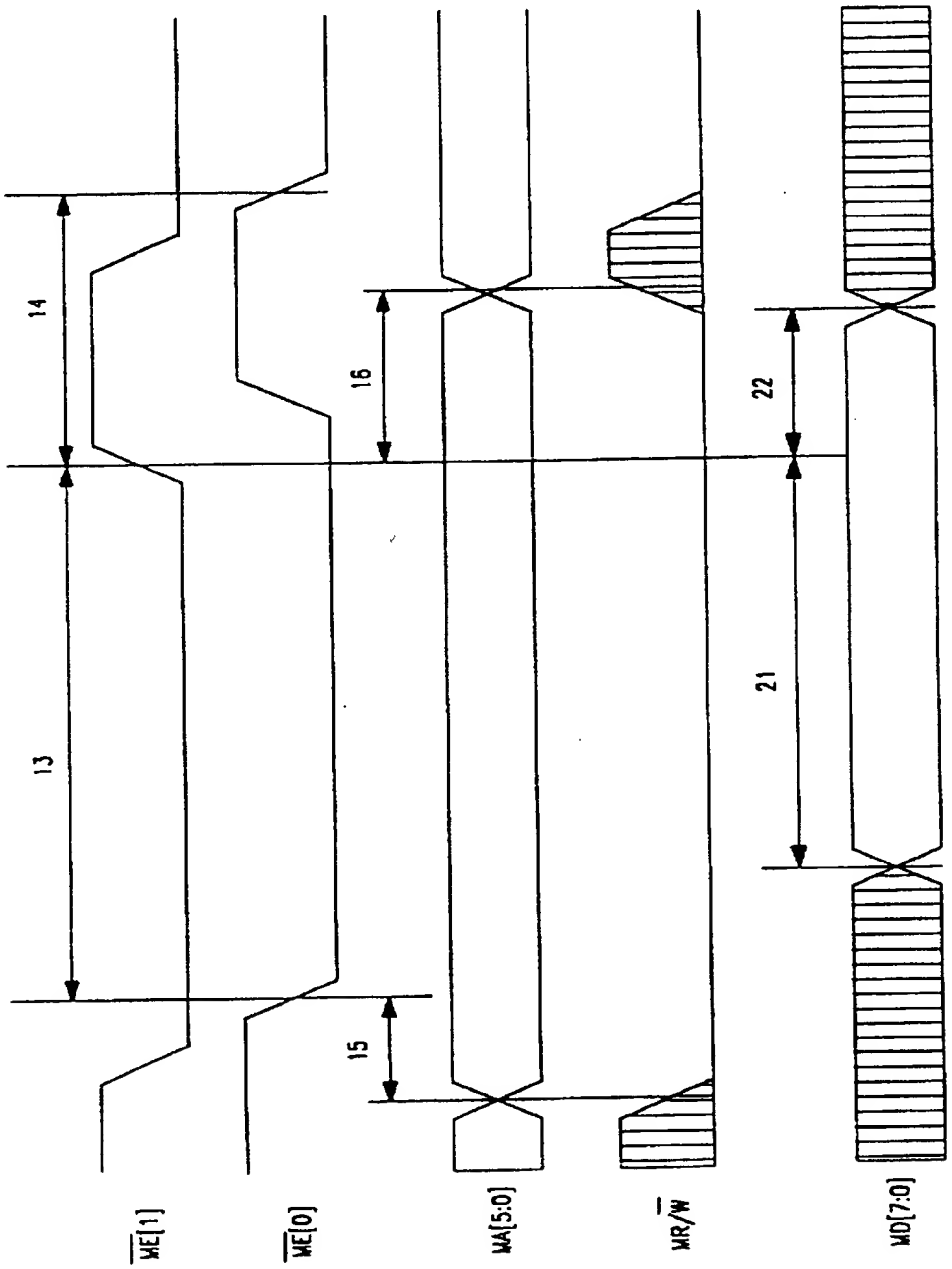


FIG. 124

	Document ID	U	Title	Current OR
59	US 6122592 A	☒	Navigation apparatus with enhanced positional display function	701/201
60	US 6121634 A	☒	Nitride semiconductor light emitting device and its manufacturing method	257/86
61	US 6115812 A	☒	Method and apparatus for efficient vertical SIMD computations	712/300
62	US 6094656 A	☒	Data exchange system comprising portable data processing units	707/100
63	US 6072667 A	☒	Method and apparatus for analysis of magnetic characteristics of magnetic device, magnetic head, and magnetic recording and reproducing apparatus	360/110
64	US 6052690 A	☒	Coherent data structure with multiple interaction contexts for a smart card	707/101
65	US 6041404 A	☒	Dual function system and method for shuffling packed data elements	712/210
66	US 6038212 A	☒	Method and system for optimizing the connection set up time in high speed communication networks for recovering from network failure	370/216
67	US 6032170 A	☒	Long instruction word controlling plural independent processor operations	708/620
68	US 6023759 A	☒	System for observing internal processor events utilizing a pipeline data path to pipeline internally generated signals representative of the event	712/227
69	US 6023147 A	☒	Hand held computerized data collection terminal with rechargeable battery pack sensor and battery power conservation	320/114
70	US 6014147 A	☒	Computer machine architecture for creating images from graphical elements and a method of operating the architecture	345/620
71	US 6011919 A	☒	Method of providing efficiency to a graphical programming language with alternative form determination and cost of execution estimation	717/114
72	US 6008812 A	☒	Image output characteristic setting device	345/418
73	US 5990830 A	☒	Serial pipelined phase weight generator for phased array antenna having subarray controller delay equalization	342/368
74	US 5938719 A	☒	Navigation apparatus with enhanced positional display function	701/207
75	US 5936677 A	☒	Microbuffer used in synchronization of image data	348/512
76	US 5920541 A	☒	Data disc having both data and data retrieval information stored thereon and method for retrieving data recorded on the data disc	369/275.3
77	US 5915067 A	☒	Multimedia optical disc facilitating branch reproduction to parental lock sections using reduced control information and a reproducing device for said disc	386/70
78	US 5909588 A	☒	Processor architecture with divisional signal in instruction decode for parallel storing of variable bit-width results in separate memory locations	712/23
79	US 5909562 A	☒	Backup FIFO in-line storage	710/310
80	US 5907691 A	☒	Dual pipelined interconnect	710/305
81	US 5907658 A	☒	Multimedia optical disk, reproduction apparatus and method for achieving variable scene development based on interactive control	386/95

VIDEO DECOMPRESSION

This application is a divisional of U.S. application Ser. No. 08/473,813 filed on Jun. 7, 1995.

INTRODUCTION

The present invention relates generally to a new and improved system for decoding a plurality of audio and video signals and, more particularly, to a new and improved system for decoding a plurality of MPEG audio and video signals.

A serial pipeline processing system of the present invention comprises a single two-wire bus used for carrying unique and specialized interactive interfacing tokens, in the form of control tokens and data tokens, to a plurality of adaptive decompression circuits and the like positioned as a reconfigurable pipeline processor.

PRIOR ART

U.S. Pat. No. 5,111,292 discloses an apparatus for encoding/decoding a HDTV signal for e.g. terrestrial transmission includes a priority selection processor for parsing compressed video codewords between high and low priority channels for transmission. A compression circuit responsive to high definition video source signals provides hierarchically layered codewords CW representing compressed video data and associated codewords T. defining the types of data represented by codewords CW. The priority selection processor, responsive to the codewords CW and T, counts the number of bits in predetermined blocks of data and determines the number of bits in each block to be allocated to the respective channels. Thereafter the processor parses the codewords CW into high and low priority codeword sequences wherein the high and low priority codeword sequences correspond to compressed video data of relatively greater and lesser importance to image reproduction respectively.

One prior art system is described in U.S. Pat. No. 5,216,724. The apparatus comprises a plurality of compute modules, in a preferred embodiment, for a total of four compute modules coupled in parallel. Each of the compute modules has a processor, dual port memory, scratch-pad memory, and an arbitration mechanism. A first bus couples the compute modules and a host processor. The device comprises a shared memory which is coupled to the host processor and to the compute modules with a second bus.

U.S. Pat. No. 4,785,349 discloses a full motion color digital video signal that is compressed, formatted for transmission, recorded on compact disc media and decoded at conventional video frame rates. During compression, regions of a frame are individually analyzed to select optimum fill coding methods specific to each region. Region decoding time estimates are made to optimize compression thresholds. Region descriptive codes conveying the size and locations of the regions are grouped together in a first segment of a data stream. Region fill codes conveying pixel amplitude indications for the regions are grouped together according to fill code type and placed in other segments of the data stream. The data stream segments are individually variable length coded according to their respective statistical distributions and formatted to form data frames. The number of bytes per frame is withered by the addition of auxiliary data determined by a reverse frame sequence analysis to provide an average number selected to minimize pauses of the compact disc during playback, thereby avoiding unpredictable seek mode latency periods characteristic of compact discs. A decoder includes a variable length decoder responsive to statistical information in the code stream for separately variable length decoding individual segments of the data stream. Region location data is derived from region descriptive data and applied with region fill codes to a plurality of region specific decoders selected by detection of the fill code type (e.g., relative, absolute, dyad and DPCM) and decoded region pixels are stored in a bit map for subsequent display.

U.S. Pat. No. 4,922,341 discloses a method for scene-model-assisted reduction of image data for digital television signals, whereby a picture signal supplied at time is to be coded, whereby a predecessor frame from a scene already coded at time t−1 is present in an image store as a reference, and whereby the frame-to-frame information is composed of an amplification factor, a shift factor, and an adaptively acquired quad-tree division structure. Upon initialization of the system, a uniform, prescribed gray scale value or picture half-tone expressed as a defined luminance value is written into the image store of a coder at the transmitter and in the image store of a decoder at the receiver store, in the same way for all picture elements (pixels). Both the image store in the coder as well as the image store in the decoder are each operated with feed back to themselves in a manner such that the content of the image store in the coder and decoder can be read out in blocks of variable size, can be amplified with a factor greater than or less than 1 of the luminance and can be written back into the image store with shifted addresses, whereby the blocks of variable size are organized according to a known quad tree data structure.

U.S. Pat. No. 5,122,875 discloses an apparatus for encoding/decoding an HDTV signal. The apparatus includes a compression circuit responsive to high definition video source signals for providing hierarchically layered codewords CW representing compressed video data and associated codewords T, defining the types of data represented by the codewords CW. A priority selection circuit, responsive to the codewords CW and T, parses the codewords CW into high and low priority codeword sequences wherein the high and low priority codeword sequences correspond to compressed video data of relatively greater and lesser importance to image reproduction respectively. A transport processor, responsive to the high and low priority codeword sequences, forms high and low priority transport blocks of high and low priority codewords, respectively. Each transport block includes a header, codewords CW and error detection check bits. The respective transport blocks are applied to a forward error check circuit for applying additional error check data. Thereafter, the high and low priority data are applied to a modem wherein quadrature amplitude modulates respective carriers for transmission.

U.S. Pat. No. 5,146,325 discloses a video decompression system for decompressing compressed image data wherein odd and even fields of the video signal are independently compressed in sequences of intraframe and interframe compression modes and then interleaved for transmission. The odd and even fields are independently decompressed. During intervals when valid decompressed odd/even field data is not available, even/odd field data is substituted for the unavailable odd/even field data. Independently decompressing the even and odd fields of data and substituting the opposite field of data for unavailable data may be used to advantage to reduce image display latency during system start-up and channel changes.

U.S. Pat. No. 5,168,356 discloses a video signal encoding system that includes apparatus for segmenting encoded video data into transport blocks for signal transmission. The

	Document ID	U	Title	Current OR
82	US 5898689 A	☒	Packet network interface	370/232
83	US 5892960 A	☒	Method and computer system for processing a set of data elements on a sequential processor	712/7
84	US 5880740 A	☒	System for manipulating graphical composite image composed of elements selected by user from sequentially displayed members of stored image sets	345/629
85	US 5878054 A	☒	Method and apparatus for test data generation	714/739
86	US 5860019 A	☒	Data driven information processor having pipeline processing units connected in series including processing portions connected in parallel	712/26
87	US 5859789 A	☒	Arithmetic unit	708/603
88	US 5819101 A	☒	Method for packing a plurality of packed data elements in response to a pack instruction	712/22
89	US 5806068 A	☒	Document data processor for an object-oriented knowledge management system containing a personal database in communication with a packet processor	707/103 R
90	US 5802519 A	☒	Coherent data structure with multiple interaction contexts for a smart card	707/100
91	US 5793756 A	☒	Method and apparatus for organizing and recovering information communicated in a radio communication system	370/311
92	US 5790867 A	☒	Compiler with extended redundant copy elimination	717/155
93	US 5778250 A	☒	Method and apparatus for dynamically adjusting the number of stages of a multiple stage pipeline	712/32
94	US 5764873 A	☒	Lazy drag of graphical user interface (GUI) objects	345/769
95	US 5745121 A	☒	Methods and apparatus for optimizing the composition of graphical elements	345/619
96	US 5742879 A	☒	Method and apparatus for reproducing documents with variable information	399/139
97	US 5724494 A	☒	Optimization method for the efficient production of images	345/592
98	US 5724258 A	☒	Neural network analysis for multifocal contact lens design	702/108
99	US 5717881 A	☒	Data processing system for processing one and two parcel instructions	712/205
100	US 5715331 A	☒	System for generation of a composite raster-vector image	382/199
101	US 5713032 A	☒	Compound document processing system	715/515
102	US 5710932 A	☒	Parallel computer comprised of processor elements having a local memory and an enhanced data transfer mechanism	712/14
103	US 5682521 A	☒	Microprocessor control system which selects operating instructions and operands in an order based upon the number of transferred executable operating instructions	712/200
104	US 5680332 A	☒	Measurement of digital circuit simulation test coverage utilizing BDDs and state bins	703/13

transport block format enhances signal recovery at the receiver by virtue of providing header data from which a receiver can determine re-entry points into the data stream on the occurrence of a loss or corruption of transmitted data. The re-entry points are maximized by providing secondary transport headers embedded within encoded video data in respective transport blocks.

U.S. Pat. No. 5,168,375 discloses a method for processing a field of image data samples to provide for one or more of the functions of decimation, interpolation, and sharpening. This is accomplished by an array transform processor such as that employed in a JPEG compression system. Blocks of data samples are transformed by the discrete even cosine transform (DECT) in both the decimation and interpolation processes, after which the number of frequency terms is altered. In the case of decimation, the number of frequency terms is reduced, this being followed by inverse transformation to produce a reduced-size matrix of sample points representing the original block of data. In the case of interpolation, additional frequency components of zero value are inserted into the array of frequency components after which inverse transformation produces an enlarged data sampling set without an increase in spectral bandwidth. In the case of sharpening, accomplished by a convolution or filtering operation involving multiplication of transforms of data and filter kernel in the frequency domain, there is provided an inverse transformation resulting in a set of blocks of processed data samples. The blocks are overlapped followed by a savings of designated samples, and a discarding of excess samples from regions of overlap. The spatial representation of the kernel is modified by reduction of the number of components, for a linear-phase filter, and zero-padded to equal the number of samples of a data block, this being followed by forming the discrete odd cosine transform (DOCT) of the padded kernel matrix.

U.S. Pat. No. 5,175,617 discloses a system and method for transmitting logmap video images through telephone line band-limited analog channels. The pixel organization in the logmap image is designed to match the sensor geometry of the human eye with a greater concentration of pixels at the center. The transmitter divides the frequency band into channels, and assigns one or two pixels to each channel, for example a 3 KHz voice quality telephone line is divided into 768 channels spaced about 3.9 Hz apart. Each channel consists of two carrier waves in quadrature, so each channel can carry two pixels. Some channels are reserved for special calibration signals enabling the receiver to detect both the phase and magnitude of the received signal. If the sensor and pixels are connected directly to a bank of oscillators and the receiver can continuously receive each channel, then the receiver need not be synchronized with the transmitter. An FFT algorithm implements a fast discrete approximation to the continuous case in which the receiver synchronizes to the first frame and then acquires subsequent frames every frame period. The frame period is relatively low compared with the sampling period so the receiver is unlikely to lose frame synchrony once the first frame is detected. An experimental video telephone transmitted 4 frames per second, applied quadrature coding to 1440 pixel logmap images and obtained an effective data transfer rate in excess of 40,000 bits per second.

U.S. Pat. No. 5,185,819 discloses a video compression system having odd and even fields of video signal that are independently compressed in sequences of intraframe and interframe compression modes. The odd and even fields of independently compressed data are interleaved for transmission such that the intraframe even field compressed data occurs midway between successive fields of intraframe odd field compressed data. The interleaved sequence provides receivers with twice the number of entry points into the signal for decoding without increasing the amount of data transmitted.

U.S. Pat. No. 5,212,742 discloses an apparatus and method for processing video data for compression/decompression in real-time. The apparatus comprises a plurality of compute modules, in a preferred embodiment, for a total of four compute modules coupled in parallel. Each of the compute modules has a processor, dual port memory, scratch-pad memory, and an arbitration mechanism. A first bus couples the compute modules and host processor. Lastly, the device comprises a shared memory which is coupled to the host processor and to the compute modules with a second bus. The method handles assigning portions of the image for each of the processors to operate upon.

U.S. Pat. No. 5,231,484 discloses a system and method for implementing an encoder suitable for use with the proposed ISO/IEC MPEG standards. Included are three cooperating components or subsystems that operate to variously adaptively pre-process the incoming digital motion video sequences, allocate bits to the pictures in a sequence, and adaptively quantize transform coefficients in different regions of a picture in a video sequence so as to provide optimal visual quality given the number of bits allocated to that picture.

U.S. Pat. No. 5,267,334 discloses a method of removing frame redundancy in a computer system for a sequence of moving images. The method comprises detecting a first scene change in the sequence of moving images and generating a first keyframe containing complete scene information for a first image. The first keyframe is known, in a preferred embodiment, as a "forward-facing" keyframe or intraframe, and it is normally present in CCITT compressed video data. The process then comprises generating at least one intermediate compressed frame, the at least one intermediate compressed frame containing difference information from the first image for at least one image following the first image in time in the sequence of moving images. This at least one frame being known as an interframe. Finally, detecting a second scene change in the sequence of moving images and generating a second keyframe containing complete scene information for an image displayed at the time just prior to the second scene change, known as a "backward-facing" keyframe. The first keyframe and the at least one intermediate compressed frame are linked for forward play, and the second keyframe and the intermediate compressed frames are linked in reverse for reverse play. The intraframe may also be used for generation of complete scene information when the images are played in the forward direction. When this sequence is played in reverse, the backward-facing keyframe is used for the generation of complete scene information.

U.S. Pat. No. 5,276,513 discloses a first circuit apparatus, comprising a given number of prior-art image-pyramid stages, together with a second circuit apparatus, comprising the same given number of novel motion-vector stages, perform cost-effective hierarchical motion analysis (HMA) in real-time, with minimum system processing delay and/or employing minimum system processing delay and/or employing minimum hardware structure. Specifically, the first and second circuit apparatus, in response to relatively high-resolution image data from an ongoing input series of successive given pixel-density image-data frames that occur at a relatively high frame rate (e.g., 30 frames per second), derives, after a certain processing-system delay, an ongoing

	Document ID	U	Title	Current OR
105	US 5675581 A	☒	Simulating user interference in a spread spectrum communication network	370/252
106	US 5671226 A	☒	Multimedia information processing system	370/474
107	US 5649223 A	☒	Word based text producing system	715/534
108	US 5644568 A	☒	Method and apparatus for organizing and recovering information communicated in a radio communication system	370/311
109	US 5640524 A	☒	Method and apparatus for chaining vector instructions	712/222
110	US 5619541 A	☒	Delay line separator for data bus	375/360
111	US 5617319 A	☒	Navigation apparatus with enhanced positional display function	701/207
112	US 5602841 A	☒	Efficient point-to-point and multi-point routing mechanism for programmable packet switching nodes in high speed data transmission networks	370/413
113	US 5602473 A	☒	Method and apparatus for analysis of magnetic characteristics of magnetic device, magnetic head, and magnetic recording and reproducing apparatus	324/209
114	US 5598547 A	☒	Vector processor having functional unit paths of differing pipeline lengths	712/222
115	US 5596570 A	☒	System and method for simulating interference received by subscriber units in a spread spectrum communication network	370/252
116	US RE35311 E	☒	Data dependency collapsing hardware apparatus	708/521
117	US 5517584 A	☒	Method and apparatus for high-speed implementation of scaling, dithering, and data remapping operations with a single processor	382/276
118	US 5515303 A	☒	Hand-held computerized data collection terminal with rechargeable battery pack sensor and battery power conservation	361/683
119	US 5481103 A	☒	Packet bar code with data sequence encoded in address/data packets	235/494
120	US 5475680 A	☒	Asynchronous time division multiplex switching system	370/412
121	US 5440687 A	☒	Communication protocol for handling arbitrarily varying data strides in a distributed processing environment	709/236
122	US 5433202 A	☒	High resolution and high contrast ultrasound mammography system with heart monitor and boundary array scanner providing electronic scanning	600/444
123	US 5412697 A	☒	Delay line separator for data bus	375/360
124	US 5315708 A	☒	Method and apparatus for transferring data through a staging memory	711/119
125	US 5297255 A	☒	Parallel computer comprised of processor elements having a local memory and an enhanced data transfer mechanism	712/14
126	US 5287449 A	☒	Automatic program generation method with a visual data structure display	345/161
127	US 5261412 A	☒	Method of continuously monitoring blood pressure	600/485

output series of successive given pixel-density vector-data frames that occur at the same given frame rate. Each vector-data frame is indicative of image motion occurring between each pair of successive image frames.

U.S. Pat. No. 5,283,646 discloses a method and apparatus for enabling a realtime video encoding system to accurately deliver the desired number of bits per frame, while coding the image only once, updates the anqutization step size used to quantize coefficients which describe, for example, an image to be transmitted over a communications channel. The data is divided into sectors, each sector including a plurality of blocks. The blocks are encoded, for example, using DCT coding, to generate a sequence of coefficients for each block. The coefficients can be quantized, and depending upon the quantization step, the number of bits required to describe the data will vary significantly. At the end of the transmission of each sector of data, the accumulated actual number of bits expended is compared with the accumulated desired number of bits expended, for a selected number of sectors associated with the particular group of data. The system then readjusts the quantization step size to target a final desired number of data bits for a plurality of sectors, for example describing an image. Various methods are described for updating the quantization step size and determining desired bit allocations.

U.S. Pat. No. 5,287,420 discloses a method and apparatus for image compression suitable for personal computer applications, which compresses and stores data in two steps. An image is captured in realtime and compressed using an efficient method and stored to a hard-disk. At some later time, the data is further compressed in non-realtime using a computationally more intense algorithm that results in a higher compression ratio. The two-step approach allows the storage reduction benefits of a highly sophisticated compression algorithm to be achieved without requiring the computational resources to perform this algorithm in realtime. A compression algorithm suitable for performing the first compression step on a host processor in a personal computer is also described. The first compression step accepts 4:2:2 YCrCb data from the video digitizer. The two chrominance components are averaged and a pseudo-random number is added to all components. The resulting values are quantized and packed into a single 32-bit word representing a 2×2 array of pixels. The seed value for the pseudo-random number is remembered so that the pseudo-random noise can be removed before performing the second compression step

U.S. Pat. No. 5,289,577 discloses a method and apparatus for a sequential process-pipeline which has a first processing stage coupled to a CODEC through a plurality of buffers, including an image data input buffer, an image data output buffer and an address buffer. The address buffer stores addresses, each of which identifies an initial address of a block of addresses within an image memory. Each block of addresses in the image memory stores a block of decompressed image data. A local controller is responsive to the writing of an address into the address buffer to initiate the operation of the CODEC to execute a Discrete Cosine Transformation Process and a Discrete Cosine Transformation Quantization Process.

The article, Chong, Yong M., *A Data-Flow Architecture for Digital Image Processing*, Wescon Technical Papers: No. 2 October/November 1984, discloses a real-time signal processing system specifically designed for image processing. More particularly, a token based data-flow architecture is disclosed wherein the tokens are of a fixed one word width having a fixed width address field. The system contains a plurality of identical flow processors connected in a ring fashion. The tokens contain a data field, a control field and a tag. The tag field of the token is further broken down into a processor address field and an identifier field. The processor address field is used to direct the tokens to the correct data-flow processor, and the identifier field is used to label the data such that the data-flow processor knows what to do with the data. In this way, the identifier field acts as an instruction for the data-flow processor. The system directs each token to a specific data-flow processor using a module number (MN). If the MN matches the MN of the particular stage, then the appropriate operations are performed upon the data. If unrecognized, the token is directed to an output data bus.

The article, Kimori, S. et al. *An Elastic Pipeline Mechanism by Self-Timed Circuits*, IEEE J. of Solid-State Circuits, Vol. 23, No 1 , February 1988, discloses an elastic pipeline having self-timed circuits. The asynchronous pipeline comprises a plurality of pipeline stages. Each of the pipeline stages consists of a group of input data latches followed by a combinatorial logic circuit that carries out logic operations specific to the pipeline stages. The data latches are simultaneously supplied with a triggering signal generated by a data-transfer control circuit associated with that stage. The data-transfer control circuits are interconnected to form a chain through which send and acknowledge signal lines control a hand-shake mode of data transfer between the successive pipeline stages. Furthermore, a decoder is generally provided in each stage to select operations to be done on the operands in the present stage. It is also possible to locate the decoder in the preceding stage in order to predecode complex decoding processing and to alleviate critical path problems in the logic circuit. The elastic nature of the pipeline eliminates any centralized control since all the interworkings between the submodules are determined by a completely localized decision and, in addition, each submodule can autonomously perform data buffering and self-timed data-transfer control at the same time. Finally, to increase the elasticity of the pipeline, empty stages are interleaved between the occupied stages in order to ensure reliable data transfer between the stages.

Accordingly, those skilled in the art have recognized a long felt need for a new and improved video decompression system obviating the deficiencies of the prior art systems. The present invention clearly fulfills this need.

SUMMARY OF INVENTION

Briefly, and in general terms, the present invention provides a new and improved method and apparatus particularly adapted for use in a two-wire pipeline system having various control and DATA tokens. The major elements of the system may include a Start Code Detector, a Video Parser incorporating a Huffman Decoder and a Microprogrammable State Machine (MSM), an Inverse Discrete Cosine Transform (IDCT), a synchronous DRAM controller with an associated address generation unit, appropriate prediction circuitry and display circuitry which includes upsampling and video timing generation.

More importantly, various embodiments of the invention may include an MPEG video decompression method and apparatus utilizing a plurality of stages interconnected by a two-wire interface arranged as a pipeline processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decoder circuit is positioned in certain of the stages for recognizing certain of the tokens as

	Document ID	U	Title	Current OR
128	US 5251323 A	☒	Vector processing apparatus including timing generator to activate plural readout units and writing unit to read vector operand elements from registers for arithmetic processing and storage in vector result register	712/5
129	US 5051940 A	☒	Data dependency collapsing hardware apparatus	708/524
130	US 5038280 A	☒	Information processing apparatus having address expansion function	712/237
131	US 4974070 A	☒	Colorgraphic reproduction system	358/500
132	US 4899232 A	☒	Apparatus for recording and/or reproducing digital data information	360/48
133	US 4890310 A	☒	Spectral type radiation imaging system	378/82
134	US 4849905 A	☒	Method for optimized RETE pattern matching in pattern-directed, rule-based artificial intelligence production systems	706/48
135	US 4825363 A	☒	Apparatus for modifying microinstructions of a microprogrammed processor	712/211
136	US 4796201 A	☒	Stored program controlled system for creating and printing graphics bearing packaging	345/585
137	US 4779192 A	☒	Vector processor with a synchronously controlled operand fetch circuits	712/8
138	US 4770182 A	☒	NMR screening method	600/410
139	US 4701044 A	☒	Image recording apparatus for composing plural partial original images into a single composite image	399/7
140	US 4661900 A	☒	Flexible chaining in vector processor with selective use of vector registers as operand and result registers	712/4
141	US 4651274 A	☒	Vector data processor	712/8
142	US 4586175 A	☒	Method for operating a packet bus for transmission of asynchronous and pseudo-synchronous signals	370/449
143	US 4504900 A	☒	Sequence instruction display system	700/26
144	US 4459664 A	☒	Multiprocessor computer system with dynamic allocation of multiprocessing tasks and processor for use in such multiprocessor computer system	709/105
145	US 4425630 A	☒	Sequence instruction display system	700/12
146	US 4371898 A	☒	Composite information recording apparatus	358/300
147	US 4266242 A	☒	Television special effects arrangement	348/588
148	US 4152765 A	☒	Programmer unit for N/C systems	700/183
149	US 4128880 A	☒	Computer vector register processing	712/4

control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token. A wide variety of unique supporting subsystem circuitry and processing techniques are disclosed for implementing the system, including memory addressing, transforming data using a common processing block, time synchronization, asynchronous swing buffering, storing of video information, a parallel Huffman decoder, and the like.

By way of example, and not necessarily by way of limitation, the present invention may include among its various features an apparatus for synchronizing time having, a time stamp for determining presentation time, a clock reference for initializing system time in a first circuit, a first time counter in communication with the clock reference for keeping system time in a first circuit and a second time counter initialized by the clock reference in a second circuit synchronized with the first time counter, for keeping a local copy of the system time and for determining the presentation timing error between the local copy of system time and system time by comparing the time stamp to the second time counter. It further includes an apparatus for synchronizing a system decoder and a video decoder using a time stamp for determining display time, a clock reference for initializing system time in the system decoder, a first time counter in communication with the clock reference for keeping system time in the system decoder and a second time counter initialized by the clock reference in the video decoder synchronized with the first time counter, for keeping a local copy of system time and for determining the display timing error between the local copy of system time and system time by comparing the time stamp to the second time counter.

Still another embodiment of the invention includes an apparatus for synchronizing a first circuit and a second circuit using a clock reference for initializing system time in the first circuit, a first circuit having a time counter in communication with the clock reference for keeping system time, a first elementary stream time counter in the first circuit for providing elementary stream time. The first circuit is adapted to receive a time stamp, and the first circuit generates synchronization time by adding elementary stream time to the time stamp and subtracting system time. The second circuit is adapted to receive synchronization time from the first circuit and has a second elementary stream time counter in synchronization with the first elementary stream time counter for providing a local copy of the elementary stream time and for determining a timing error between the system time and the time stamp by comparing synchronization time to the local copy of elementary stream time. In this way, the clock reference signal does not have to be passed directly to the second circuit in order to determine the timing error.

In another embodiment of the invention, an apparatus for synchronizing a first circuit and a second circuit has a clock reference for initializing system time in the first circuit. The first circuit has a time counter in communication with the clock reference for keeping system time, and a first video time counter for providing video decoding time. The first circuit is adapted to receive a video time stamp and subtracting system time. The second circuit is adapted to receive synchronization time from the first circuit and has a second video time counter in synchronization with the first video time counter for providing a local copy of video decoding time and for determining a timing error between system time and the video time stamp by comparing synchronization time to the local copy of video decoding time. Accordingly, the clock reference signal does not have to be passed directly to the second circuit in order to determine the timing error.

The present invention also includes a method for providing timing information by providing a video data stream having a time stamp carried in packet header wherein the time stamp refers to the first picture in the packet of data. In the next step a register is provided having a flag used to indicate valid time stamp information which is taken from the packet header and placed into the register. Next, the time stamp is removed from the video data stream and placed in the register. Next, the method encounters a picture start and subsequently examines the status of the register to determine if valid time stamp information is contained in the register by checking the flag status. A time stamp is generated in response to the picture start if the flag indicates valid time stamp information is contained in the register and then the time stamp is inserted back into the data stream.

Another embodiment of the invention includes an apparatus described above wherein the elementary stream time counters are restricted to 16 bits. Likewise, there is an apparatus as described above, wherein the second elementary stream time counter located in the elementary stream decoder is restricted to 16 bits. Furthermore, there is an apparatus as described above wherein the synchronization time is restricted to 16 bits for controlling the elementary stream decoder.

The present invention also has a process for decoding video and for determining display time errors against a threshold value. It then parses video data into tokens for further processing, determining if a time stamp token is indicated, comparing the time stamp token to a video time, and generates a compared value to determine an indicative of timing error. Next, it determines whether the compared value, when compared against a threshold value, is within acceptable parameters when a timing error is indicated and indicates when the compared value is outside acceptable parameters.

An alternative embodiment of the invention includes an apparatus for using a system decoder and a video decoder. The system decoder is adapted to accept MPEG system streams and demultiplexing video data and the video time stamp from the stream. The system decoder has a first time counter representative of system time. The video decoder accepts the video data and the video time stamp, and has a second time counter in synchronization with the first time counter. The video decoder also has a decoder buffer for accepting the video data at a substantially constant rate and outputting the video data at a varying rate and for passing a video time stamp. The video decoder while decoding a picture from the video data also compares the video time stamp for the decoded picture with the second time counter to determine the appropriate display time. There is also a method for determining a timing error between a first circuit and a second circuit by providing the first circuit with a system time (SY), a time stamp (TS), and an elementary stream time (ET), obtaining synchronization time (X) by using the elementary stream time (ET), the time stamp (TS), and the system time (SY), in accordance with the equation X=ET+TS−SY, providing synchronization time (X) to the second circuit and generating a synchronized elementary stream time (ET2) and obtaining a timing error by using synchronized time (X) and in accordance with the equation ET2−X. Hence, the first circuit can be time synchronized with the second circuit without passing system time to the second circuit.

Another method for determining a timing error between a first circuit and a second circuit has the following steps:

	Document ID	U	Title	Current OR
150	US 3633179 A	☐	INFORMATION HANDLING SYSTEMS FOR ELIMINATING DISTINCTIONS BETWEEN DATA ITEMS AND PROGRAM INSTRUCTIONS	707/1

providing the first circuit with a time stamp (TS), and an initial time (IT), obtaining a synchronization time (X) by using the time stamp (TS) and the initial time (IT), in accordance with the equation X=TS−1, providing synchronization time (X) to the second circuit and generating a synchronized elementary stream time (ET) and obtaining a timing error by using synchronized time (X) and in accordance with the equation ET−X. In this way, the first circuit can be time synchronized with the second circuit without passing system time to the second circuit.

Still another method for determining a timing error between a first circuit and a second circuit includes the following steps: providing the first circuit with a system time (SY), a video time stamp (VTS), and a video decoding time (VT), obtaining synchronization time (X) by using the video decoding time (VT), the video time stamp (VTS) and the system time (SY), in accordance with the equation X=VT+VTS−SY, providing synchronization time (X) to the second circuit and generating a video decoding time (VT2) in the second circuit which is synchronized to the video decoding time (VT) in the first circuit, and obtaining a time error by using synchronized time (X) and in accordance with the equation VT2−X. Accordingly, the first circuit can be time synchronized with the second circuit without passing system time to the second circuit.

In accordance with the present invention, the parallel Huffman decoder block will decode MPEG Huffman coded Variable Length Codes (VLCs) and Fixed Length Codes (FLCs), and pass through tokens under the control of the parser microprogrammable state Machine (MSM), and can sustain a high throughput.

In one embodiment of the invention a code lookup technique is employed to decode Huffman codes to achieve performance requirements and to handle the second MPEG-2 transform coefficient table which is irregular or non-canonical in nature. Practice of the invention also facilitates decoding certain more complex components from the stream in a single cycle without the assistance of an external controller. Examples of such complex components are Escape-coded coefficients, Intra-DC values and Motion Vector deltas, all of which are present in the stream as combined VLC/FLC components.

To decode a VLC, input is first loaded into the two input data registers handling most significant and least significant data. A selector is used to align the beginning of the next VLC with the ROM input. Hence, for a very first VLC, the selector outputs the top 28 bits of its 59-bit input and the top 16 bits of these are passed to a Huffman Code ROM For subsequent VLCs, the selector effectively shifts the input according to the total count of bits decoded thus far, the count is maintained by adding the size of each VLC, as it is decoded, to a running total. The various word widths are a result of the maximum coded size which can be decoded, which is the 28-bit MPEG-1 Escape Coded Coefficient, and the maximum VLC size which is 16 bits (DCT coefficient tables).

The "table select" input is used to select between the various different Huffman code tables required by MPEG.

The ROM has addresses which are controlled with a selector/shifter. The ROM performs a VLC table index calculation, followed by the index-to-data operation that yields decoded data.

The index calculation is a content addressable memory (CAM) operation with "don't care" matching implemented to handle the Huffman codes which form the presented data. Since the index generation is performed in a look-up manner (rather than algorithmically) there is no restriction to handling tables which are canonical.

The ROM address of the present invention is in two fields. The larger field is the bit-pattern to be decoded, and the smaller field selects which Huffman code table is to be examined. In addition to the complete MPEG code tables, the ROM also has entries to identify illegal VLC patterns, which exist for some code tables.

In another embodiment of the invention, a procedure is used for providing a word with fixed width, having a fixed number of bits to be used for addressing variable width data, and having a width defining field and address field. There is also a procedure for addressing memory with a fixed width word, having a fixed number of bits, to be used for addressing data and having a substitution field and an address field, and an apparatus for addressing memory, including a state machine and an arithmetic core.

The procedure for addressing memory is characterized by providing a fixed width word having a predetermined fixed number of bits to be used for addressing variable width data, defining the fixed width word with a width defining field and an address field, providing the width defining field with at least one bit to serve as the termination marker, defining the address field with a plurality of bits defining the address of data, varying the size of bits in the address field in inverse relation to the size of the variable width data, varying the number of bits in the width defining field in direct relation to the size of the variable width data, and maintaining a fixed width word for addressing variable width data while varying the width of the width defining field and the address field.

The procedure for addressing memory may also include defining the address field with a plurality of bits defining the address of the data, defining a variable width substitution field with a least one substitution bit, the substitution field having at least one bit to serve as a termination marker between the address field and the substitution field, using the substitution field to indicate substituted bits from a separate addressing source, and maintaining a fixed width word for addressing variable width data while inversely varying the width of the address field and the width of the substitution field.

In accordance with the invention, a process for addressing variable width data in a memory may be characterized by providing a memory having words of predetermined width and composed of partial words, rotating the partial word to be accessed to a least significant bit justification, extending the remaining part of the word so that the accessed word will be recognized as a partial word, restoring the remaining part of the word, and rotating the word until the partial word is restored to its original position.

The invention may also include a method and apparatus for addressing memory wherein a word is provided with fixed width, having a fixed number of bits to be used for addressing variable width data, and having a width defining field and address field. In addition, a procedure for addressing memory with a fixed width word, having a fixed number of bits, to be used for addressing data and having a substitution field and an address field, may be used.

The invention may also include a method of accessing from RAM a number M of words that is less than the predetermined fixed burst length N of the RAM, the RAM including an enable line that selectably enables and disables reading from and writing to the RAM, the method comprising the steps of:

ordering N words to be read from or written to the RAM;

determining when M words have been read from or written to the RAM, M being less than N; and

	Document ID	U	Title	Current OR
1	US 20030223381 A1	☐	Method for controlling parties in real-time data communication	370/285
2	US 20030221089 A1	☒	Microprocessor data manipulation matrix module	712/221
3	US 20030189947 A1	☒	Routing and rate control in a universal transfer mode network	370/428
4	US 20030144810 A1	☒	Methods and apparatus for data analysis	702/108
5	US 20030048466 A1	☒	Image reading device, method of controlling the same, control program, storage medium and image forming apparatus provided with the image reading device	358/1.12
6	US 20030043810 A1	☒	System and method for communicating data using a common switch fabric	370/395.1
7	US 20030028657 A1	☒	Directly addressed multicast protocol	709/230
8	US 20030026252 A1	☒	Data packet structure for directly addressed multicast protocol	370/390
9	US 20020180931 A1	☒	Method for determining vision defects and for collecting data for correcting vision defects of the eye by interaction of a patient with an examiner and apparatus therefor	351/211
10	US 20020163905 A1	☒	Remote control system	370/347
11	US 20020124803 A1	☒	System for optimising the production performance of a milk producing animal herd	119/14.08
12	US 20020105940 A1	☒	Resource allocation in packet-format communication	370/349
13	US 20020105917 A1	☒	Method and apparatus for packet-based media communication	370/260
14	US 20020095529 A1	☒	Screening of data packets in a gateway	709/330
15	US 20020060976 A1	☒	Optical pickup device with a plurality of laser couplers	369/121
16	US 20020054147 A1	☒	GRAPHIC DATA PROCESSING APPARATUS USING DISPLAYED GRAPHICS FOR APPLICATION PROGRAM SELECTION	345/810
17	US 20020054145 A1	☒	GRAPHIC DATA PROCESSING APPARATUS USING DISPLAYED GRAPHICS FOR PROGRAM SELECTION	345/810

HPS Trailer Page
for

Walk-Up_Printing

UserID: d

Printer: cpk2_2c21_gbkbptr

Summary

Document	Pages	Printed	Missed	Copies
US006542988	14	14	0	1
US005717883	22	22	0	1
US005758051	16	16	0	1
US005915117	13	13	0	1
US005918005	23	23	0	1
US006006317	23	23	0	1
US006112019	79	79	0	1
Total (7)	190	190	0	-

	Document ID	U	Title	Current OR
18	US 20020015485 A1	☒	Service and information management system for a telecommunications network	379/220.01
19	US 20020002586 A1	☒	Methods and apparatus for creating and hosting customized virtual parties via the internet	709/205
20	US 6658235 B1	☒	Method for transmitting control information in a communication system	455/67.13
21	US 6557146 B1	☒	Method for the comparison of electrical circuits	716/3
22	US 6484255 B1	☒	Selective writing of data elements from packed data based upon a mask using predication	712/224
23	US 6384781 B1	☒	Method and apparatus for calibrating a remote system which employs coherent signals	342/368
24	US 6246684 B1	☒	Method and apparatus for re-ordering data packets in a network environment	370/394
25	US 6181766 B1	☒	Digital encoding of RF computerized tomography data	378/15
26	US 6134272 A	☒	Data input/output apparatus of transport decoder	375/240.27
27	US 6121903 A	☒	On-the-fly data re-compression	341/63
28	US 6119216 A	☒	Microprocessor capable of unpacking packed data in response to a unpack instruction	712/22
29	US 5951624 A	☒	Computer system to compress pixel bits	708/203
30	US 5917981 A	☒	Digital scan mammography apparatus utilizing velocity adaptive feedback and method	378/98.8
31	US 5765142 A	☒	Method and apparatus for the development and implementation of an interactive customer service system that is dynamically responsive to change in marketing decisions and environments	705/26
32	US 5675526 A	☒	Processor performing packed data multiplication	708/620
33	US 5651120 A	☒	Graphic data processing apparatus using displayed graphics for application program selection	345/821
34	US 5502800 A	☒	Graphic data processing apparatus using displayed graphics for application program selection	345/619
35	US 5423016 A	☒	Block buffer for instruction/operand caches	711/123
36	US 5422879 A	☒	Data flow control mechanism utilizing low level flow control codes	370/236
37	US 5391865 A	☒	Optical pickup apparatus and optical grating assembly therefor	250/201.5
38	US 5339603 A	☒	Method for setting a folding station included in an apparatus for preparing items to be mailed, and apparatus for preparing items to be mailed and folding station adapted for carrying out such method	53/429
39	US 5337402 A	☒	Graphic data processing apparatus using displayed graphics for application program selection	345/619

US005644742A

United States Patent [19]

Shen et al.

[11] Patent Number: 5,644,742

[45] Date of Patent: Jul. 1, 1997

[54] **PROCESSOR STRUCTURE AND METHOD FOR A TIME-OUT CHECKPOINT**

[75] Inventors: **Gene W. Shen**, Mountain View; **John Szeto**, Oakland; **Niteen A. Patkar**, Sunnyvale, all of Calif.; **Michael C. Shebanow**, Plano, Tex.

[73] Assignee: **Hal Computer Systems, Inc.**, Campbell, Calif.

[21] Appl. No.: **473,223**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 398,299, Mar. 3, 1995, abandoned, which is a continuation of Ser. No. 390,885, Feb. 14, 1995, abandoned.

[51] **Int. Cl.**[6] **G06F 11/00**

[52] **U.S. Cl.** **395/591**; 395/183.14

[58] **Field of Search** 395/375, 591, 395/183.14

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,703,481	10/1987	Fremont .	
4,847,755	7/1989	Morrison et al. .	
4,893,233	1/1990	Denman et al. .	
4,903,264	2/1990	Talgam et al. .	
4,912,707	3/1990	Kogge et al. .	
5,003,458	3/1991	Yamaguchi et al. .	
5,003,462	3/1991	Blaner et al. .	
5,021,945	6/1991	Morrison et al. .	
5,075,844	12/1991	Jardine et al. .	
5,093,908	3/1992	Beacom et al. .	
5,193,206	3/1993	Mills .	
5,235,700	8/1993	Alaiwan et al. .	
5,261,071	11/1993	Lyon .	
5,269,017	12/1993	Hayden et al.	395/375
5,271,013	12/1993	Gleeson .	
5,293,499	3/1994	Jensen .	
5,301,309	4/1994	Sugano .	
5,313,634	5/1994	Eickemeyer .	
5,313,647	5/1994	Kaufman et al. .	
5,335,457	8/1994	Shebanow et al.	395/375
5,463,745	10/1995	Vidwans et al.	395/375
5,471,598	11/1995	Quattromani et al.	395/375
5,481,685	1/1996	Nguyen et al.	395/375
5,497,499	3/1996	Gang et al.	395/375

OTHER PUBLICATIONS

Mike Johnson, *Superscalar Microprocessor Design*, 1991.

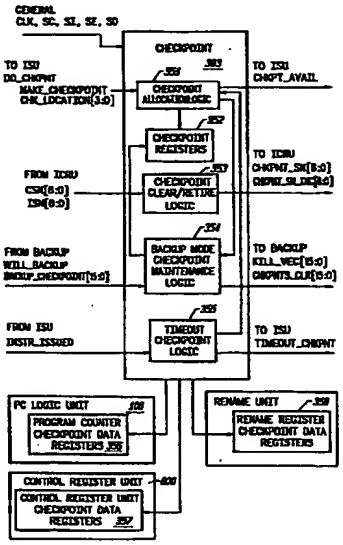
Primary Examiner—William M. Treat

Attorney, Agent, or Firm—Flehr Hohbach Test Albritton & Herbert LLP

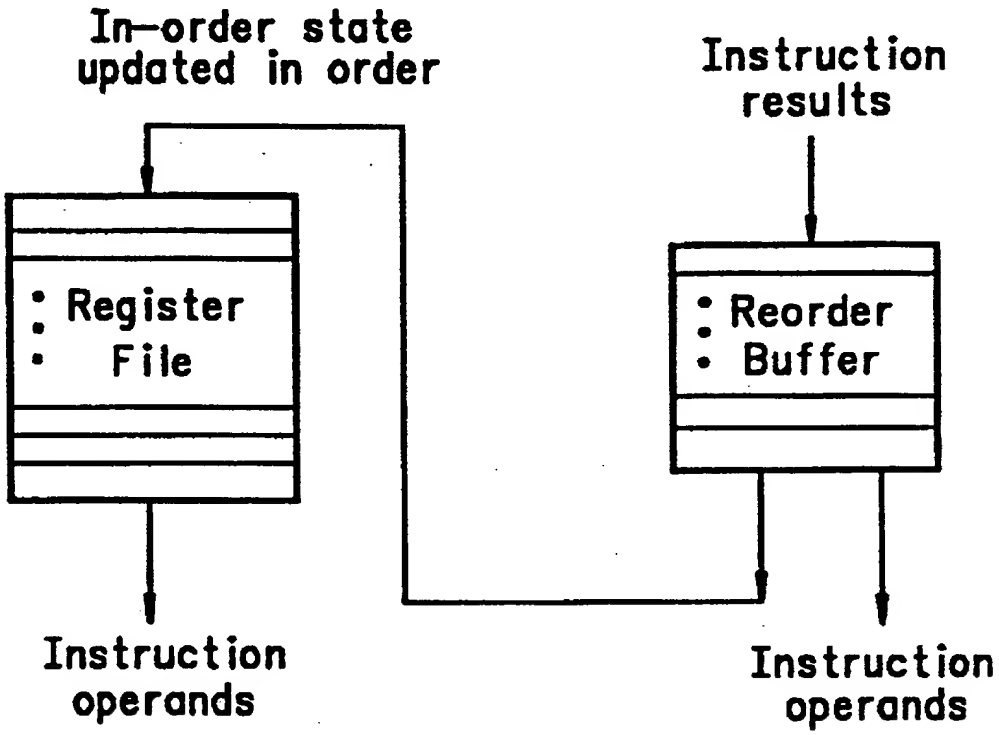
[57] **ABSTRACT**

Time-out checkpoints are formed based on a predetermined time-out condition or interval since the last checkpoint was formed rather than forming a checkpoint to store current processor state based merely on decoded Instruction attributes. Such time-out conditions may include the number of instructions issued or the number of clock cycles elapsed, for example. Time-out checkpointing limits the maximum number of instructions within a checkpoint boundary and bounds the time period for recovery from an exception condition. The processor can restore time-out based checkpointed state faster than an instruction decode based checkpoint technique in the event of an exception so long as the instruction window size is greater than the maximum number of instructions within a checkpoint boundary, end such method eliminates processor state restoration dependency on instruction window size. Time-out checkpoints may be implemented with conventional checkpoints, or in a novel logical and physical register rename map checkpointing technique. Timeout checkpoint formation may be used with conventional processor backup techniques as well as with a novel backtracking technique including processor backup and backstepping.

16 Claims, 60 Drawing Sheets



	Document ID	U	Title	Current OR
40	US 5318129 A	☒	Method and device for setting up sondes against the wall of a cased well	166/336
41	US H001296 H	☒	Optical switching device and parallel processing architecture	385/16
42	US 5289570 A	☒	Picture image editing system for forming boundaries in picture image data in a page memory device	715/521
43	US 5241533 A	☒	Packet switching network with alternate trunking function	370/227
44	US 5210743 A	☒	Switching element with multiple operating modes and switching network incorporating a plurality of such switching elements, in particular for switching asynchronous time-division multiplex packets	370/422
45	US 5079548 A	☒	Data packing circuit in variable length coder	341/67
46	US 5023824 A	☒	Hand-held computerized data collection terminal with indented hand grip and conforming battery drawer	361/680
47	US 4890624 A	☒	Fetal heart rate counting system using digital signal processing	600/453
48	US 4817121 A	☒	Apparatus for checking baggage with x-rays	378/57
49	US 4761753 A	☒	Vector processing apparatus	708/520
50	US 4760518 A	☒	Bi-directional databus system for supporting superposition of vector and scalar operations in a computer	710/107
51	US 4734805 A	☒	Magnetic head supporting mechanism	360/244.8
52	US 4565941 A	☒	Oscillatory drive mechanisms for a ring laser gyro	310/328
53	US 4511938 A	☒	Magnetizable recording disk and disk file employing servo sector head positioning	360/77.08
54	US 4441165 A	☒	Real-time ordinal-value filters utilizing complete intra-data comparisons	708/207
55	US 4203345 A	☒	Automatic visual teaching device for the learning of music or component parts thereof	84/478
56	US 4125149 A	☒	Heat exchange elements	165/10
57	US 3839000 A	☐	METHOD FOR CONTROLLING CURVATURE OF REGIONS IN A SHAPED THERMOPLASTIC SHEET	65/29.19



Reorder Buffer Organization

FIG. 1
(PRIOR ART)

	Document ID	U	Title	Current OR
1	JP 20032 23007 A	☐	METHOD FOR MAKING LITHOGRAPHIC PRINTING PLATE	
2	JP 20020 82968 A	☒	PICTURE READING SYSTEM AND PICTURE READING METHOD, AND STORAGE MEDIUM	
3	JP 20012 85094 A	☒	RADIO RECEIVER	
4	JP 20012 45017 A	☒	USB SIMULATION DEVICE AND STORAGE MEDIUM	
5	JP 20010 45278 A	☒	IMAGE PROCESSOR	
6	JP 20002 22159 A	☒	INFORMATION PROCESSOR, INFORMATION PROCESSING METHOD AND STORAGE MEDIUM STORING COMPUTER READABLE PROGRAM	
7	JP 20001 96963 A	☒	SOLID-STATE IMAGE PICKUP DEVICE	
8	JP 20001 84229 A	☒	IMAGE PROCESSOR	
9	JP 20000 90127 A	☒	JAPANESE ANALYZING DEVICE	
10	JP 11291 435 A	☒	PRINTING APPARATUS	
11	JP 10039 903 A	☒	PROGRAM DEVELOPMENT SUPPORTING DEVICE	
12	JP 07320 086 A	☒	METHOD AND DEVICE FOR IMAGE GENERATION	
13	JP 06309 363 A	☒	JAPANESE ANALYZING DEVICE	
14	JP 06006 686 A	☒	IMAGE PICKUP DEVICE	
15	JP 04199 469 A	☒	PICTURE GENERATION DEVICE FOR COMPUTER FOR CONTROL	
16	JP 04013 175 A	☒	SIMULATED VISUAL FIELD PRODUCING DEVICE FOR TRAIN OPERATION SIMULATOR	
17	JP 03022 735 A	☒	PACKET TRANSMITTER FOR VIDEO SIGNAL	
18	JP 03020 864 A	☒	INFORMATION PROCESSOR HAVING VECTOR INSTRUCTION SET FOR FUZZY CALCULATION	
19	JP 01107 731 A	☒	IMAGE SENSING APPARATUS	
20	JP 01049 164 A	☒	INFORMATION RECORDING AND REPRODUCING DEVICE	

Checkpoint State in Conventional Checkpointing Schemes

States that may be modified (mod) by Instruction A:

mod	–	–	mod	–	–	–	–	–	–

States that may be modified (mod) by Instruction B:

mod	–	–	–	–	–	–	–	–	–

States that may be modified (mod) by Instruction C:

–	mod	mod	–	mod	mod	mod	–	mod	mod

States that may be modified (mod) by Instruction D:

–	–	–	–	–	–	–	mod	–	–

Checkpointed States comprise all states that may be modified by any one of the instructions in the instruction set:

state1	state2	state3	state4	state5	state6	state7	state8	state9	state10

Conventional Checkpoint register stores all state that aray be modified by any one of the executable instructions.

FIG. 3

	Document ID	U	Title	Current OR
21	JP 63044 243 A	☒	ADDRESS ARITHMETIC UNIT	
22	JP 62159 273 A	☒	PROCESSOR FOR VECTOR INSTRUCTION	
23	JP 61062 174 A	☒	INFORMATION PROCESSOR	
24	JP 61025 275 A	☒	VECTOR INSTRUCTION PROCESSOR	
25	JP 59165 143 A	☒	DATA PROCESSOR	
26	EP 94897 9 A2	☒	Image creating apparatus, image creating method, and computer-readable recording medium containing image creating program	
27	WO 98435 86 A1	☒	TITLE DATA NOT AVAILABLE	
28	US 20030 20046 3 A	☒	Network security provision method e.g. for packet switched network, involves selectively forwarding untrusted packet from specific network element of one system to other autonomous system based on set security rules	
29	US 20030 18466 5 A	☒	Arrangement method of array of picture elements involves arranging additional set of pixels within non-uniformly spaced and non-uniformly sized gaps to reduce composite array of non-uniform pixels overlaying array of first set of pixels	
30	US 20020 11214 7 A	☒	Computer system used in 3D graphics and signal processing application, copies each data element of selected set of data elements to specified data fields located in corresponding portion of destination operand	
31	US 20020 06233 1 A	☒	Computer implemented method packed data element adding method in multimedia application, involves inserting each packet data element into one portion of partial product using corresponding partial product selector	
32	US 64249 21 B	☒	Averaged hybridization array (HA) for correct determination of average relative transcript abundance for each array element of many HAs, and novel composite HAs formed from a number of user selected different HAs	
33	EP 10795 73 A	☒	Method of managing calls over data network by selecting resource elements based on usage policy or network actual usage	
34	US 59908 30 A	☒	Operation control apparatus for phased array antenna used in terrestrial, airborne and space-borne communication networks	
35	US 57782 50 A	☒	Dynamic pipeline for microprocessor - includes control logic that controls first data selector to select either first set of data or first operation data as selected data	
36	DE 19619 058 A	☒	Hand-held calculation aid - performs entry of operands per digit, with appropriate symbol entering respective position, selected from set of all available symbols through repeated activation of same button	
37	US 58809 79 A	☒	Computer system for providing absolute difference of unsigned values - in which packed data sets are generated by subtracting between two sets of packed data elements stored in memory	
38	JP 08316 968 A	☒	Asynchronous transfer mode switch - has scheduler which controls read-out of packet frame from packet memory which stores tag part with communication path identifier and data part, together with packet selection element, in single memory address	
39	US 53393 96 A	☒	Parallel computer interconnection path selection - comparing next priority coordinate of first selected processing element with corresponding next priority coordinate of second coordinate set, and sequentially transferring data packet to next coordinate transforming crossbar switch	

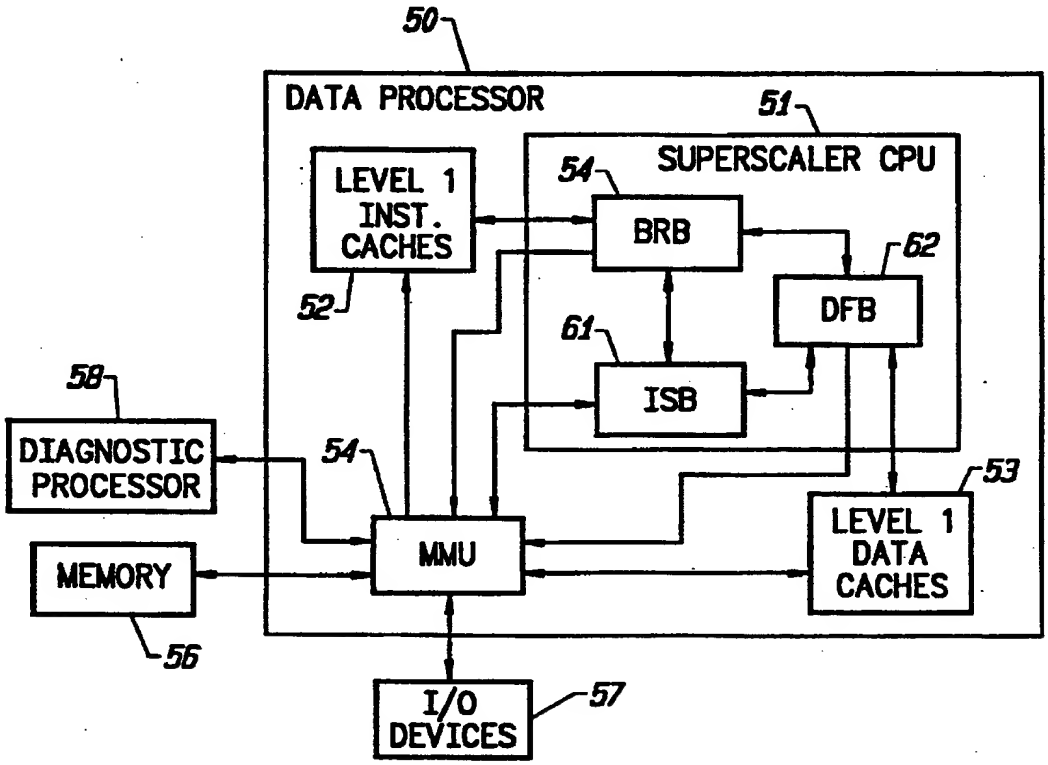

50
DATA PROCESSOR
51
SUPERSCALER CPU
LEVEL 1 INST. CACHES
52
54
BRB
62
DFB
61
ISB
58
DIAGNOSTIC PROCESSOR
54
MMU
53
LEVEL 1 DATA CACHES
MEMORY
56
I/O DEVICES
57

FIG. 4

	Document ID	U	Title	Current OR
40	EP 527366 A	☒	Variable delay circuit for use in timing generator of IC tester - has main and corrected conversion tables from which control data is selected according to detected ambient temp.	
41	EP 390555 A	☒	Reduced tape width multi-track tape recorder - controls width-wise alignment of combination head with tape using light emitters and receivers at side of tape	
42	SU 1568233 A	☒	Multi-functional logic converter for automated control system - has two extra switches with control inputs connected to output of comparator of first relay element	
43	GB 2214756 A	☒	Demultiplexion appts. for data signal receiver channels - has switching elements, receiving gate signals, connected to each other and to associated latching appts.	
44	GB 2211697 A	☒	Self-routing switching element for asynchronous time switch - includes selectors receiving tagged packet signals and arbiters outputting transmitted packet signals, having signal path connections	
45	EP 314650 A	☒	Method for artificial intelligence production - passing tokens to descendant modes upon comparison match and maintaining patterns to ancestor nodes	
46	EP 308624 A	☒	Solid state imaging device with line decimated output - has shaft register with linear part of serially connected image data holding elements connected to holding elements in carousels	
47	EP 259123 A	☒	Circular knitting machine control system - has multi-line communication bus receiving data from several control modules	
48	DE 3507703 C	☒	Data carrier mfr. method - using removal or addition of elements to matrix to make characters prior to partial encapsulation	
49	EP 171592 A	☐	Compiler optimisation by generating basis items and kill sets - for use during global common sub-expression elimination and code motion procedures	

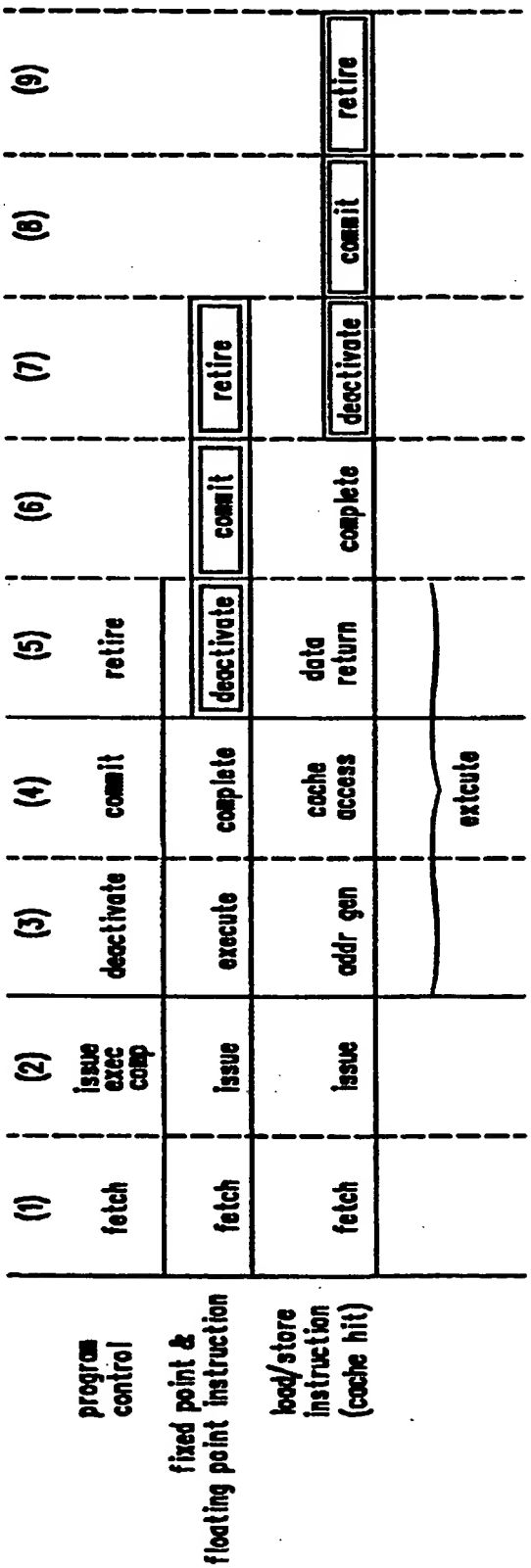

program control
fixed point & floating point instruction
load/store instruction (cache hit)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
fetch
issue exec comp
deactivate
commit
retire
issue
execute
complete
deactivate
commit
retire
fetch
issue
addr gen
cache access
data return
complete
deactivate
commit
retire
execute

FIG. 5

	L #	Hits	Search Text	DBs
1	L1	360962	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item)	USPAT; US-PGPUB
2	L2	360976	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item suboperand consituent)	USPAT; US-PGPUB
3	L3	271330	(portion part set subset) near20 (operand pack$2 composite compound)	USPAT; US-PGPUB
4	L4	1556	2 near30 3	USPAT; US-PGPUB
5	L5	325714	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near10 (element item suboperand consituent)	USPAT; US-PGPUB
6	L6	237043	(portion part set subset) near10 (operand pack$2 composite compound)	USPAT; US-PGPUB
7	L7	875	5 near20 6	USPAT; US-PGPUB
8	L11	150	7 and (operand data).ab,ti.	USPAT; US-PGPUB
9	L12	57	4 and (operand data).ab,ti. not 11	USPAT; US-PGPUB

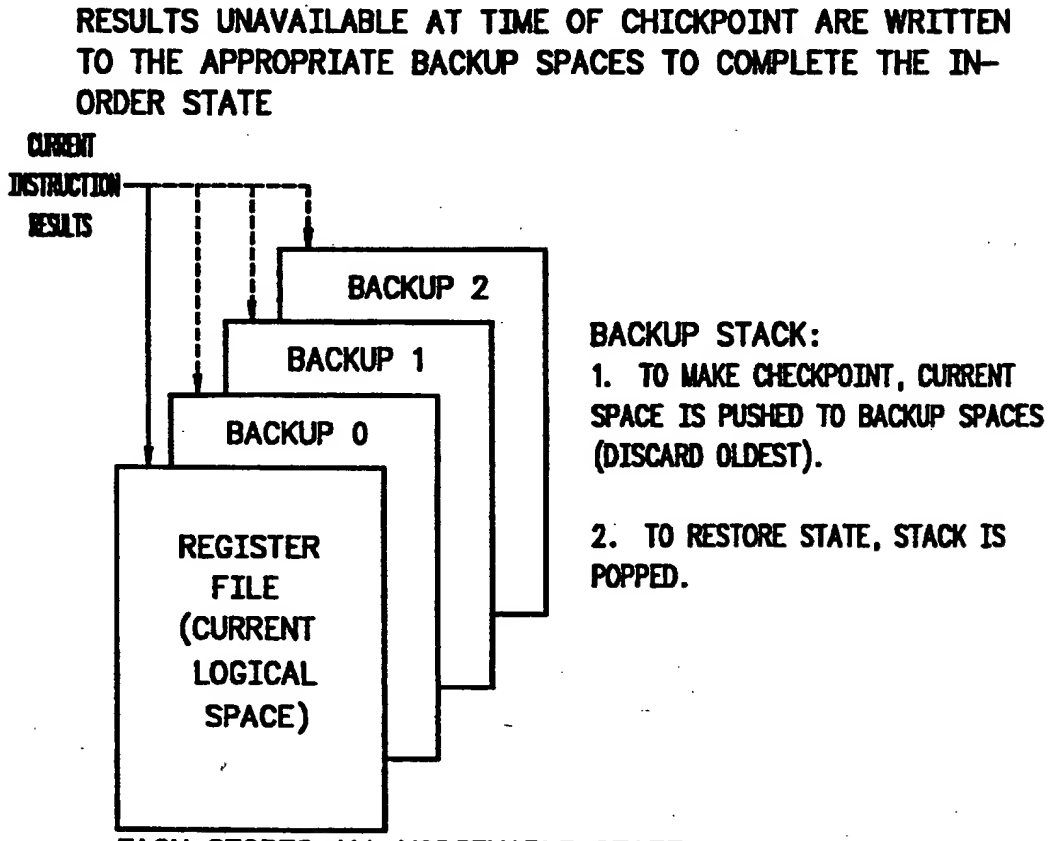


FIG. 2
(PRIOR ART)

	L #	Hits	Search Text	DBs
1	L1	360962	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item)	USPAT; US-PGPUB
2	L2	360976	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item suboperand consituent)	USPAT; US-PGPUB
3	L3	271330	(portion part set subset) near20 (operand pack$2 composite compound)	USPAT; US-PGPUB
4	L4	1556	2 near30 3	USPAT; US-PGPUB
5	L5	325714	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near10 (element item suboperand consituent)	USPAT; US-PGPUB
6	L6	237043	(portion part set subset) near10 (operand pack$2 composite compound)	USPAT; US-PGPUB
7	L7	875	5 near20 6	USPAT; US-PGPUB
8	L11	150	7 and (operand data).ab,ti.	USPAT; US-PGPUB
9	L12	57	4 and (operand data).ab,ti. not 11	USPAT; US-PGPUB
10	L13	226532	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4) near20 (element item suboperand consituent)	EPO; JPO; DERWENT; IBM_TDB
11	L14	115651	(portion part set subset) near20 (operand pack$2 composite compound)	EPO; JPO; DERWENT; IBM_TDB
12	L15	575	13 near30 14	EPO; JPO; DERWENT; IBM_TDB
13	L16	49	15 and (operand data).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
14	L18	461210	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4 reorder$3 order$3) near20 (element item)	USPAT; US-PGPUB
15	L19	343779	(portion part$5 set subset) near20 (operand pack$2 composite compound)	USPAT; US-PGPUB
16	L21	259532	(shuffl$3 reshuffl$3 arrang$3 rearrang$3 select$3 cop$4 reorder$3 order$3) near20 (element item)	EPO; JPO; DERWENT; IBM_TDB
17	L22	184472	(portion part$5 set subset) near20 (operand pack$2 composite compound)	EPO; JPO; DERWENT; IBM_TDB
18	L20	98	18 near30 19 and (operand data).ab,ti. not (11 12)	USPAT; US-PGPUB
19	L23	21	21 near30 22 and (operand data).ab,ti. not 16	EPO; JPO; DERWENT; IBM_TDB

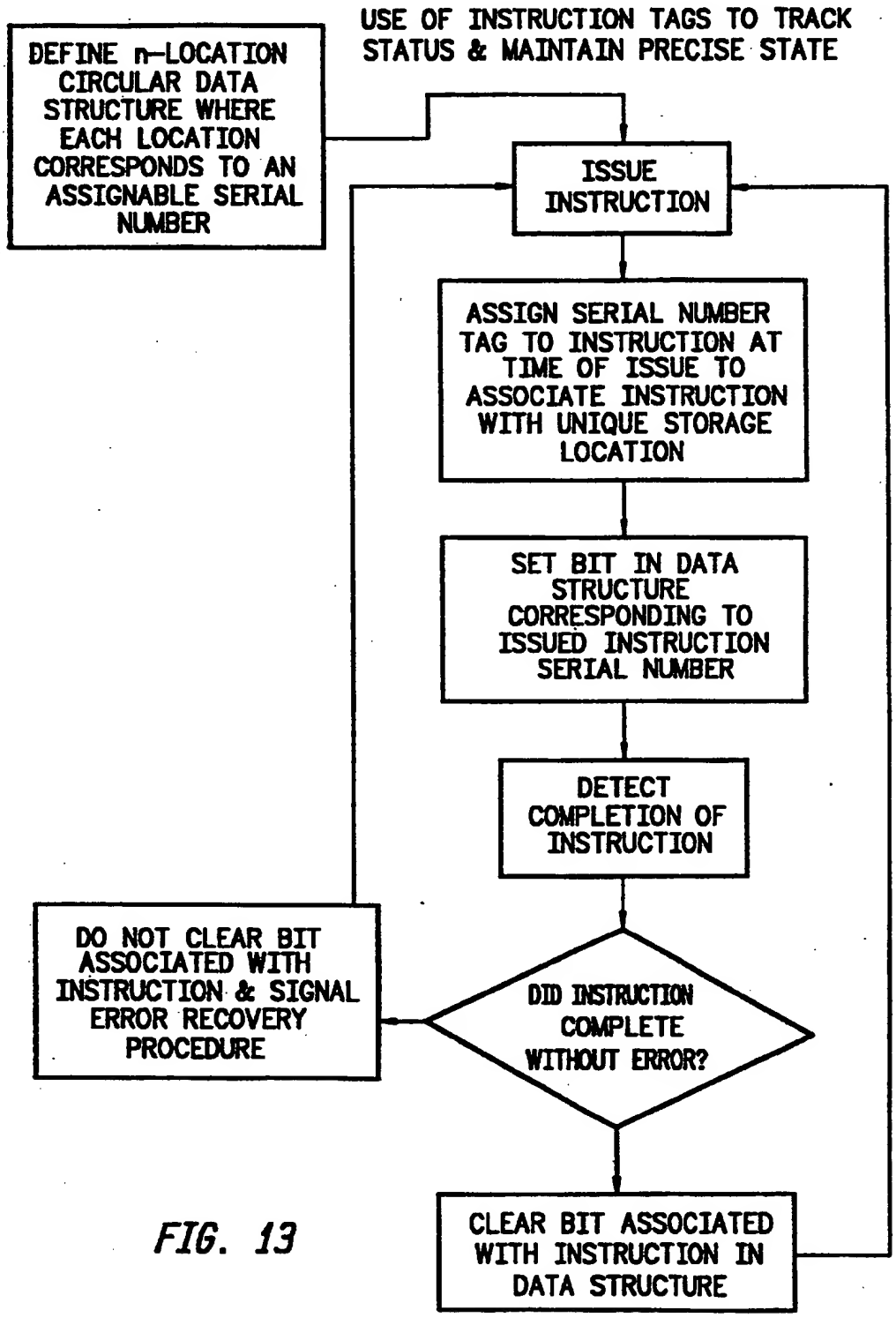

USE OF INSTRUCTION TAGS TO TRACK STATUS & MAINTAIN PRECISE STATE
DEFINE n-LOCATION CIRCULAR DATA STRUCTURE WHERE EACH LOCATION CORRESPONDS TO AN ASSIGNABLE SERIAL NUMBER
ISSUE INSTRUCTION
ASSIGN SERIAL NUMBER TAG TO INSTRUCTION AT TIME OF ISSUE TO ASSOCIATE INSTRUCTION WITH UNIQUE STORAGE LOCATION
SET BIT IN DATA STRUCTURE CORRESPONDING TO ISSUED INSTRUCTION SERIAL NUMBER
DETECT COMPLETION OF INSTRUCTION
DID INSTRUCTION COMPLETE WITHOUT ERROR?
DO NOT CLEAR BIT ASSOCIATED WITH INSTRUCTION & SIGNAL ERROR RECOVERY PROCEDURE
CLEAR BIT ASSOCIATED WITH INSTRUCTION IN DATA STRUCTURE

FIG. 13

	Document ID	U	Title	Current OR
1	US 20030208487 A1	☐	Content searching engine	707/6
2	US 20030203502 A1	☒	Near-field transform spectroscopy	436/164
3	US 20030188128 A1	☒	Executing stack-based instructions within a data processing apparatus arranged to apply operations to data items stored in registers	712/202
4	US 20030118052 A1	☒	System and method for reassembling packets in a network element	370/474
5	US 20030117678 A1	☒	Optical layer multicasting using a single sub-carrier header with active header detection, deletion, and new header insertion via opto-electrical processing	398/153
6	US 20030115441 A1	☒	Method and apparatus for packing data	712/225
7	US 20030053448 A1	☒	Systems and methods for providing differentiated services within a network communication system	370/353
8	US 20030048751 A1	☒	Dual mode service platform within network communication system	370/231
9	US 20020174228 A1	☒	Method and device for reserving transmission band on internet	709/226
10	US 20020146028 A1	☒	Optical layer multicasting using a single sub-carrier header with active header detection, deletion, and re-insertion via a circulating optical path	370/432
11	US 20020146027 A1	☒	Optical layer multicasting using a single sub-carrier header with active header detection, deletion, and insertion via reflective single sideband optical processing	370/432
12	US 20020146007 A1	☒	Optical layer multicasting using a multiple sub-carrier header and a multicast switch with active header insertion via reflective single sideband optical processing	370/390
13	US 20020146006 A1	☒	Optical layer multicasting using multiple sub-carrier headers with header detection, deletion, and insertion via reflective single sideband optical processing	370/390
14	US 20020145786 A1	☒	Optical layer multicasting using a multicast switch to effect survivablity and security	398/98
15	US 20020145785 A1	☒	Optical layer multicasting using a single sub-carrier header and an optical multicasting switch	398/98
16	US 20020145783 A1	☒	Optical layer multicasting using a multiple sub-carrier header and a multicast switch with active header insertion via single sideband optical processing	398/70
17	US 20020141409 A1	☒	Optical layer multicasting	370/390

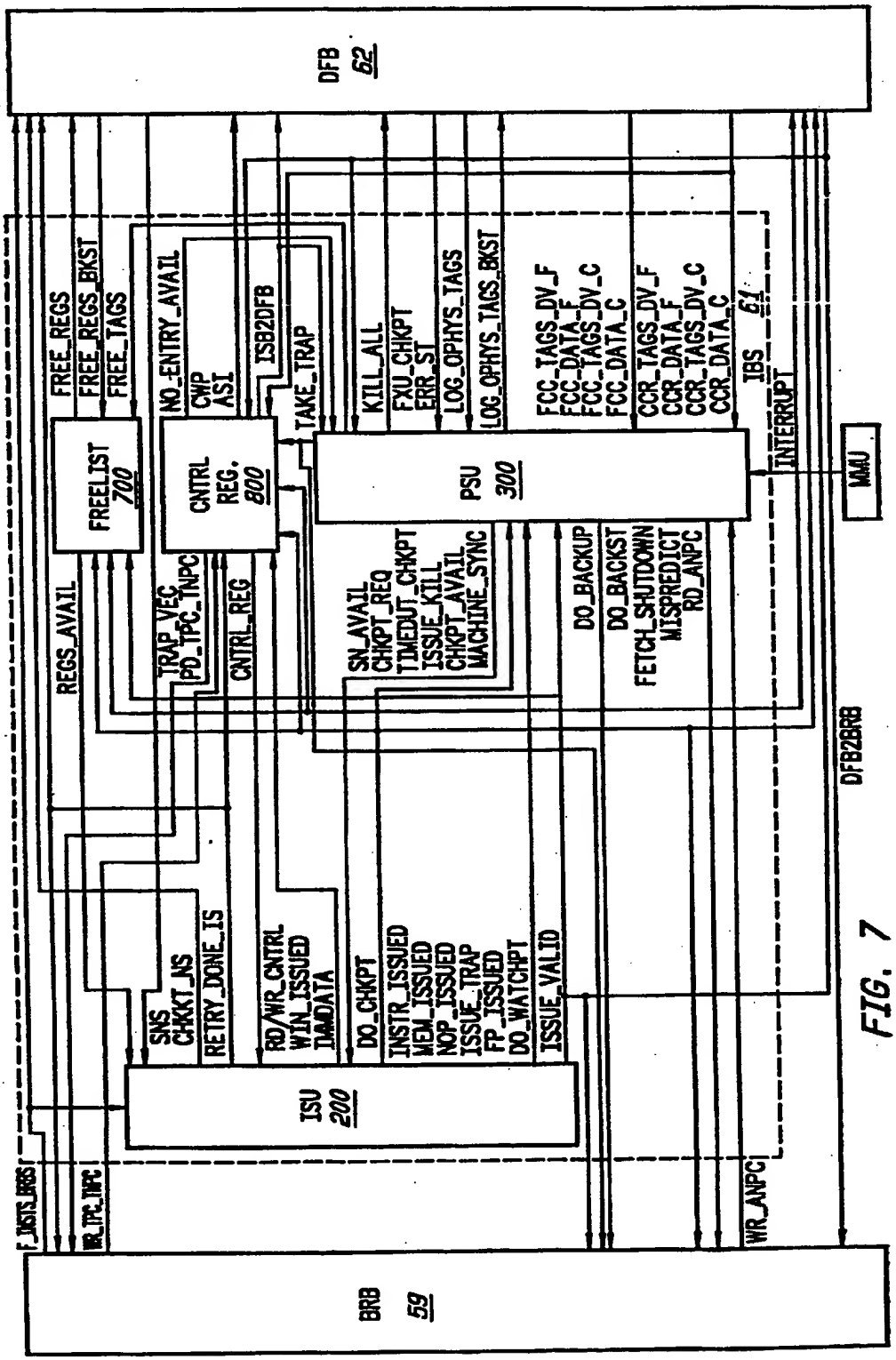

DFB 62
FREE_REGS
FREE_REGS_BKST
FREE_TAGS
NO_ENTRY_AVAIL
CWP
ASI
ISB2DFB
TAKE_TRAP
KILL_ALL
FXU_CHKPT
ERR_ST
LOG_OPHYS_TAGS
LOG_OPHYS_TAGS_BKST
FCC_TAGS_DV_F
FCC_DATA_F
FCC_TAGS_DV_C
FCC_DATA_C
CCR_TAGS_DV_F
CCR_DATA_F
CCR_TAGS_DV_C
CCR_DATA_C
IBS 61
INTERRUPT
MMU
FREELIST 700
CNTRL REG. 800
PSU 300
REGS_AVAIL
TRAP_VEC
PD_TPC_TNPC
CNTRL_REG
SN_AVAIL
CHKPT_REQ
TIMEOUT_CHKPT
ISSUE_KILL
CHKPT_AVAIL
MACHINE_SYNC
DO_BACKUP
DO_BACKST
FETCH_SHUTDOWN
MISPREDICT
RD_ANPC
D/FB2BRB
SNS
CHKKT_NS
RETRY_DONE_IS
RD/WR_CNTRL
WIN_ISSUED
IMMDATA
DO_CHKPT
INSTR_ISSUED
MEM_ISSUED
NOP_ISSUED
ISSUE_TRAP
FP_ISSUED
DO_WATCHPT
ISSUE_VALID
ISU 200
WR_ANPC
BRB 59

FIG. 7

	Document ID	U	Title	Current OR
18	US 20020 14140 8 A1	☒	Optical layer multicasting using multiple sub-carrier headers with header detection, deletion, and insertion via transmit single sideband optical processing	370/390
19	US 20020 14101 9 A1	☒	Optical layer multicasting using a single sub-carrier header and a multicast switch with active header insertion via single sideband optical processing	398/101
20	US 20020 14101 8 A1	☒	Optical layer multicasting using a single sub-carrier header and a multicast switch with active header insertion	398/101
21	US 20020 14101 7 A1	☒	Optical layer multicasting switch	398/101
22	US 20020 14101 5 A1	☒	Optical layer multicasting using a single sub-carrier header and a multicast switch with active header insertion via reflective single sideband optical processing	398/98
23	US 20020 14101 4 A1	☒	Optical layer multicasting using a multiple sub-carrier header and multicasting switch	398/70
24	US 20020 13136 4 A1	☒	Handling of data packets	370/230
25	US 20020 09772 4 A1	☒	Processing of data packets within a network element cluster	370/392
26	US 20020 06858 8 A1	☒	Wireless base station and packet transfer apparatus for dynamically controlling data transmission rate	455/461
27	US 20020 01694 3 A1	☒	Code structure, encoder, encoding method, and associated decoder and decoding method and iteratively decodable code structure, encoder, encoding method, and associated iterative decoder and iterative decoding method	714/755
28	US 20020 01084 7 A1	☒	Executing partial-width packed data instructions	712/22
29	US 20010 04314 6 A1	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	340/855 .8
30	US 20010 04261 7 A1	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/65. 1
31	US 20010 04202 3 A1	☒	Product fulfillment system	705/26
32	US 20010 03328 1 A1	☒	Three-dimensional CAD system and recording medium for three-dimensional CAD system	345/420
33	US 20010 01772 3 A1	☒	High-throughput, low-latency next generation internet networks using optical label switching and high-speed optical header generation, detection and reinsertion	398/82
34	US 20010 01341 1 A1	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/65. 1

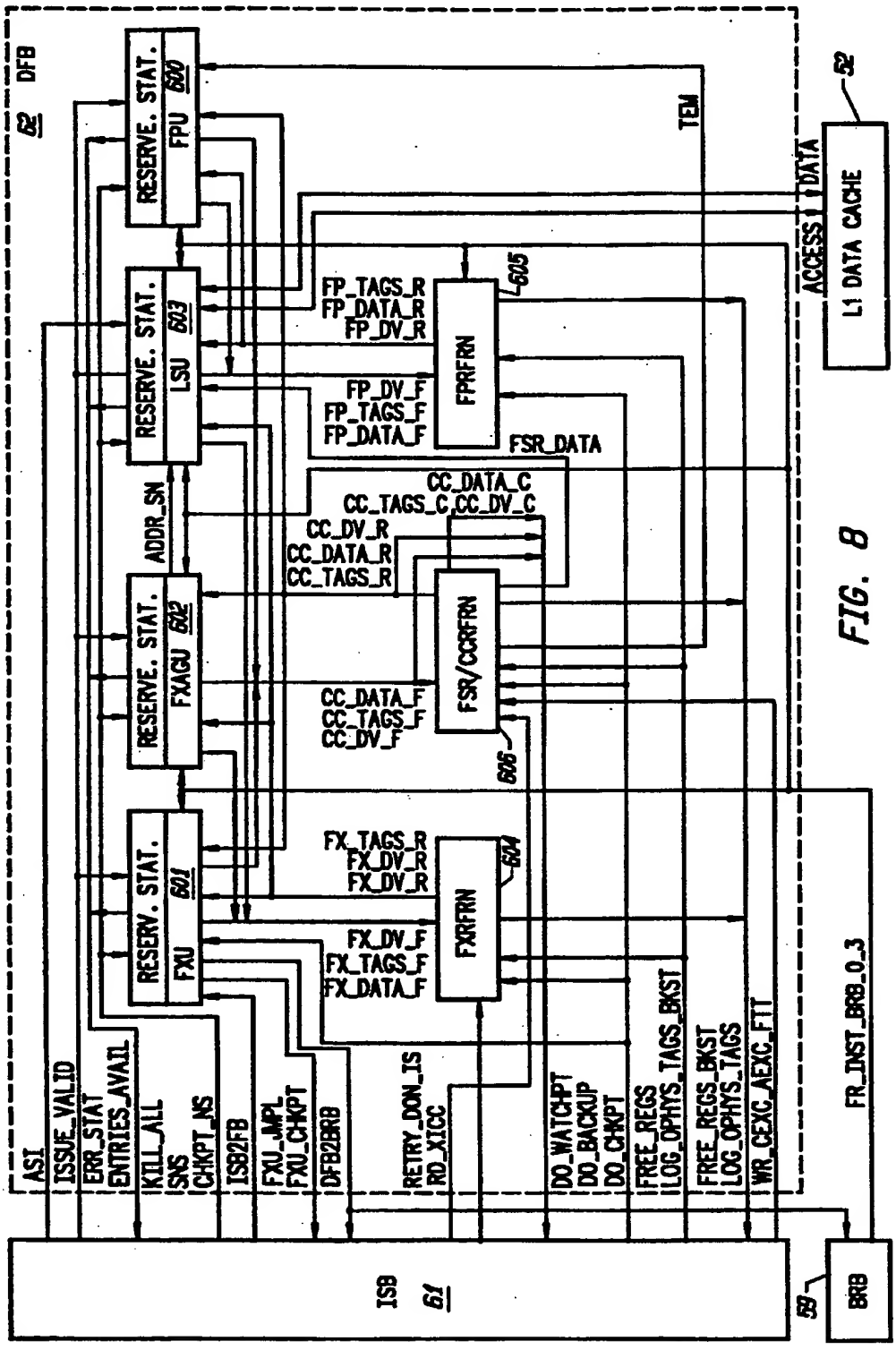

62 DFB
RESERVE. STAT.
FPU 600
RESERVE. STAT.
LSU 603
RESERVE. STAT.
FXAGU 602
RESERV. STAT.
FXU 601
ADDR_SN
FP_TAGS_R
FP_DATA_R
FP_DV_R
FP_DV_F
FP_TAGS_F
FP_DATA_F
FPRFRN
605
FSR_DATA
CC_DATA_C
CC_TAGS_C
CC_DV_C
CC_DV_R
CC_DATA_R
CC_TAGS_R
FSR/CCRFRN
CC_DATA_F
CC_TAGS_F
CC_DV_F
606
FX_TAGS_R
FX_DV_R
FX_DV_R
FXRFRN
604
FX_DV_F
FX_TAGS_F
FX_DATA_F
TEM
52
ACCESS DATA
L1 DATA CACHE
ASI
ISSUE_VALID
ERR_STAT
ENTRIES_AVAIL
KILL_ALL
SNS
CHKPT_NS
ISB2FB
FXU_MPL
FXU_CHKPT
DFB2BRB
RETRY_DON_IS
RD_XICC
DO_WATCHPT
DO_BACKUP
DO_CHKPT
FREE_REGS
LOG_OPHYS_TAGS_BKST
FREE_REGS_BKST
LOG_OPHYS_TAGS
WR_CEXC_AEXC_FTT
FR_INST_BRB_0_3
ISB 61
59
BRB

FIG. 8

	Document ID	U	Title	Current OR
35	US 20010 01341 0 A1	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/65.1
36	US 66577 57 B1	☒	High-throughput low-latency next generation internet network using optical label switching and high-speed optical header generation detection and reinsertion	
37	US 66313 89 B2	☒	Apparatus for performing packed shift operations	708/209
38	US 66115 22 B1	☒	Quality of service facility in a device for performing IP forwarding and ATM switching	370/395.21
39	US 65885 05 B2	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/250.17
40	US 65805 37 B1	☒	High-throughput, low-latency next generation internet networks using optical label switching and high-speed optical header generation, detection and reinsertion	398/79
41	US 65713 01 B1	☒	Multi processor system and FIFO circuit	710/31
42	US 65708 48 B1	☒	System and method for congestion control in packet-based communication networks	370/230.1
43	US 65457 81 B1	☒	High-throughput, low-latency next generation internet networks using optical label switching and high-speed optical header generation, detection and reinsertion	398/51
44	US 65258 51 B2	☒	High-throughput, low-latency next generation internet networks using optical label switching and high-speed optical header generation, detection and reinsertion	398/166
45	US 65258 50 B1	☒	High-throughput, low-latency next generation internet networks using optical label switching and high-speed optical header generation, detection and reinsertion	398/49
46	US 65224 35 B1	☒	High-throughput, low-latency next generation internet networks using optical label switching and high-speed optical header generation, detection and reinsertion	398/49
47	US 64972 80 B2	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/250.07
48	US 64815 05 B2	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/387
49	US 64183 91 B1	☒	Testing system for performing an operation of an application which controls testing equipment for testing a device under test and method for controlling the same	702/123
50	US 63595 69 B2	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	340/856.3
51	US 63436 49 B1	☒	Methods and associated apparatus for downhole data retrieval, monitoring and tool actuation	166/250.01
52	US 63398 19 B1	☒	Multiprocessor with each processor element accessing operands in loaded input buffer and forwarding results to FIFO output buffer	712/16
53	US 62719 46 B1	☒	Optical layer survivability and security system using optical label switching and high-speed optical header generation and detection	398/79
54	US 62330 75 B1	☒	Optical layer survivability and security system	398/79
55	US 62302 53 B1	☒	Executing partial-width packed data instructions	712/22
56	US 62197 75 B1	☒	Massively parallel computer including auxiliary vector processor	712/11

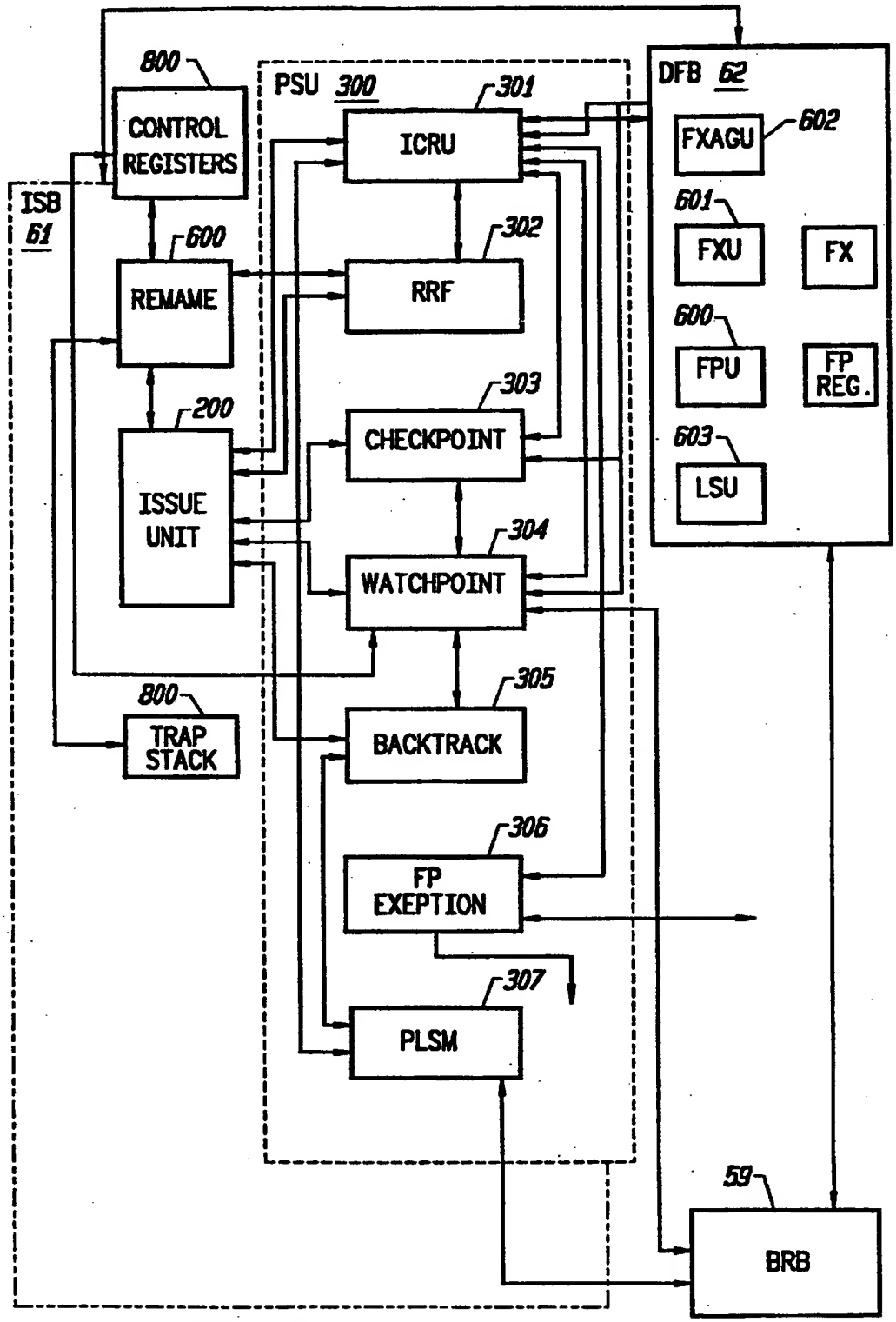

800
CONTROL REGISTERS
ISB 61
600
REMAME
200
ISSUE UNIT
800
TRAP STACK
PSU 300
301
ICRU
302
RRF
303
CHECKPOINT
304
WATCHPOINT
305
BACKTRACK
306
FP EXEPTION
307
PLSM
DFB 62
602
FXAGU
601
FXU
FX
600
FPU
FP REG.
603
LSU
59
BRB

FIG. 9

	Document ID	U	Title	Current OR
57	US 6219161 B1	☒	Optical layer survivability and security system	398/79
58	US 6192467 B1	☒	Executing partial-width packed data instructions	712/222
59	US 6160651 A	☒	Optical layer survivability and security system using optical label switching and high-speed optical header reinsertion	398/79
60	US 6122725 A	☒	Executing partial-width packed data instructions	712/200
61	US 6111673 A	☒	High-throughput, low-latency next generation internet networks using optical tag switching	398/79
62	US 6101513 A	☒	Method and apparatus for displaying database information according to a specified print layout and page format	715/527
63	US 6091689 A	☒	Optical pickup device with a plurality of laser couplers	369/112.21
64	US 6078869 A	☒	Method and apparatus for generating more accurate earth formation grid cell property information for use by a simulator to display more accurate simulation results of the formation near a wellbore	702/6
65	US 6075539 A	☒	Method and apparatus for displaying CAD geometric object and storage medium storing geometric object display processing programs	345/419
66	US 6074111 A	☒	Printing system, photographing apparatus, printing apparatus and combining method	400/76
67	US 6018497 A	☒	Method and apparatus for generating more accurate earth formation grid cell property information for use by a simulator to display more accurate simulation results of the formation near a wellbore	367/72
68	US 6005855 A	☒	Method and apparatus for providing variable rate data in a communications system using statistical multiplexing	370/335
69	US 5936955 A	☒	Network for mutually connecting computers and communicating method using such network	370/389
70	US 5926643 A	☒	Data driven processor performing parallel scalar and vector processing	712/7
71	US 5907842 A	☒	Method of sorting numbers to obtain maxima/minima values with ordering	707/7
72	US 5872987 A	☒	Massively parallel computer including auxiliary vector processor	712/3
73	US 5835492 A	☒	Network for mutually connecting computers and communicating method using such network	370/389
74	US 5815421 A	☒	Method for transposing a two-dimensional array	708/520
75	US 5793661 A	☒	Method and apparatus for performing multiply and accumulate operations on packed data	708/603
76	US 5757432 A	☒	Manipulating video and audio signals using a processor which supports SIMD instructions	348/384.1
77	US 5689647 A	☒	Parallel computing system with processing element number setting mode and shortest route determination with matrix size information	712/11
78	US 5677862 A	☒	Method for multiplying packed data	708/620

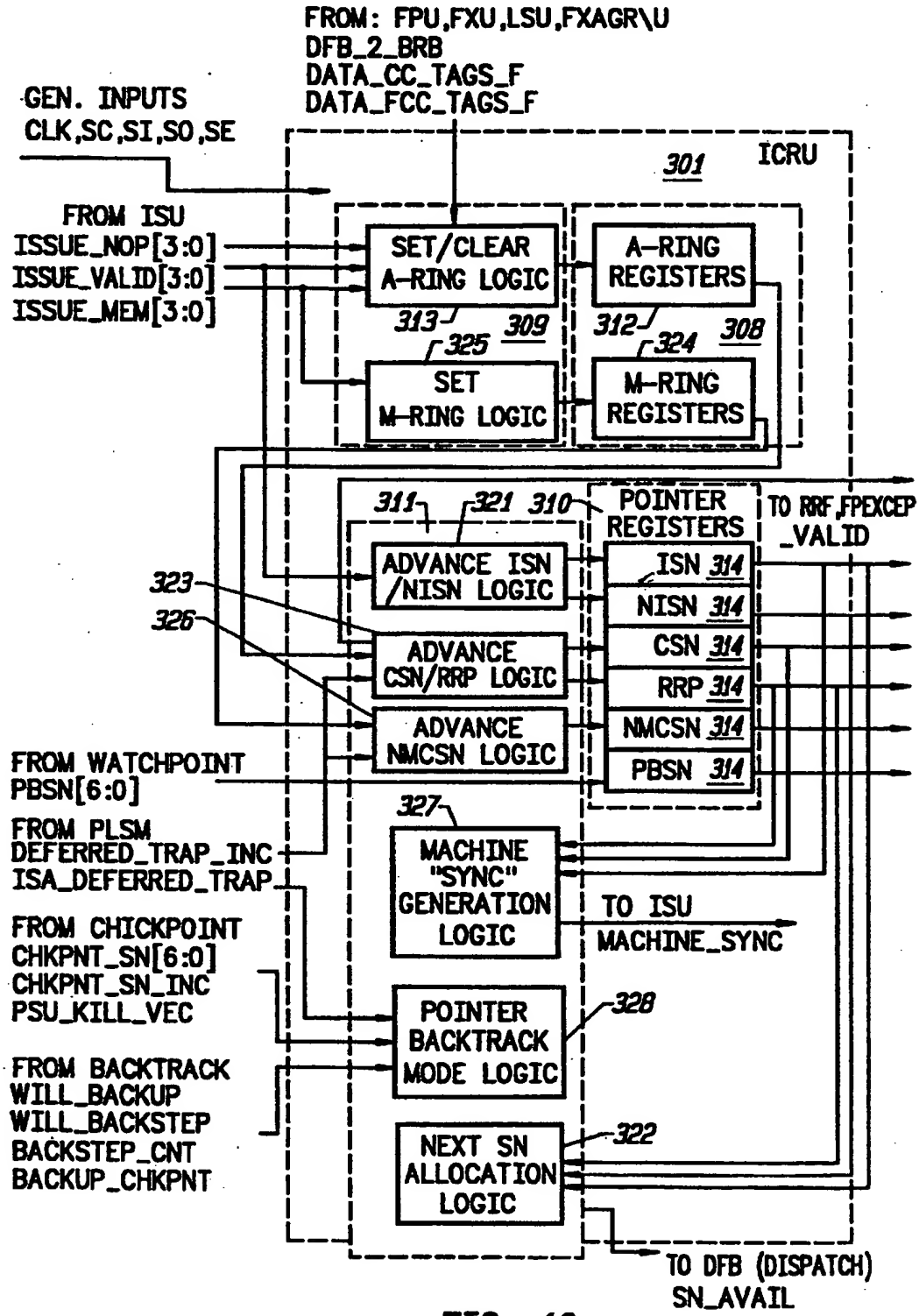

FROM: FPU,FXU,LSU,FXAGR\U
DFB_2_BRB
DATA_CC_TAGS_F
DATA_FCC_TAGS_F
GEN. INPUTS
CLK,SC,SI,SO,SE
301
ICRU
FROM ISU
ISSUE_NOP[3:0]
ISSUE_VALID[3:0]
ISSUE_MEM[3:0]
SET/CLEAR A-RING LOGIC
A-RING REGISTERS
313
309
312
308
325
324
SET M-RING LOGIC
M-RING REGISTERS
311
321
310
POINTER REGISTERS
TO RRF,FPEXCEP_VALID
ADVANCE ISN /NISN LOGIC
ISN 314
NISN 314
CSN 314
RRP 314
NMCSN 314
PBSN 314
323
326
ADVANCE CSN/RRP LOGIC
ADVANCE NMCSN LOGIC
FROM WATCHPOINT
PBSN[6:0]
327
FROM PLSM
DEFERRED_TRAP_INC
ISA_DEFERRED_TRAP
MACHINE "SYNC" GENERATION LOGIC
TO ISU
MACHINE_SYNC
FROM CHICKPOINT
CHKPNT_SN[6:0]
CHKPNT_SN_INC
PSU_KILL_VEC
POINTER BACKTRACK MODE LOGIC
328
FROM BACKTRACK
WILL_BACKUP
WILL_BACKSTEP
BACKSTEP_CNT
BACKUP_CHKPNT
NEXT SN ALLOCATION LOGIC
322
TO DFB (DISPATCH)
SN_AVAIL

FIG. 10

	Document ID	U	Title	Current OR
79	US 5623685 A	☒	Vector register validity indication to handle out-of-order element arrival for a vector computer with variable memory latency	712/9
80	US 5574933 A	☒	Task flow computer architecture	712/28
81	US 5361681 A	☒	Program controlled cooking system using video data collection	99/331
82	US 5315508 A	☒	Label generating and data tracking system for processing purchase orders	705/28
83	US 5208806 A	☒	ISDN terminal equipment operating with circuit switching mode and packet switching mode	370/352
84	US 5166927 A	☒	Adaptive pathfinding neutral network for a packet communication system	370/238
85	US 5151830 A	☒	Magnetic recording and reproducing apparatus and method of recording and reproducing	360/32
86	US 5113521 A	☒	Method and apparatus for handling faults of vector instructions causing memory management exceptions	714/15
87	US 5097364 A	☒	Magnetic recording and reproducing apparatus and method of recording and reproducing	360/32
88	US 5072377 A	☒	Data driven processor with data pairing apparatus combining a hash memory with counter directional data loops	711/216
89	US 5043867 A	☒	Exception reporting mechanism for a vector processor	712/222
90	US 5008812 A	☒	Context switching method and apparatus for use in a vector processing system	712/228
91	US 4949250 A	☒	Method and apparatus for executing instructions for a vector processing system	712/208
92	US 4866668 A	☒	Multiple memory loading system based on multilevel lists	711/148
93	US 4823258 A	☒	Index limited continuous operation vector processor	712/9
94	US 4771380 A	☒	Virtual vector registers for vector processing system	712/6
95	US 4638496 A	☒	Secure reliable transmitting and receiving system for transfer of digital data	375/351
96	US 4484304 A	☒	Transaction execution system having keyboard and message customization, improved key function versatility and message segmentation	345/733
97	US 4319336 A	☒	Transaction execution system with improved key function versatility	705/21
98	US 3866030 A	☐	Two's complement parallel array multiplier	708/625

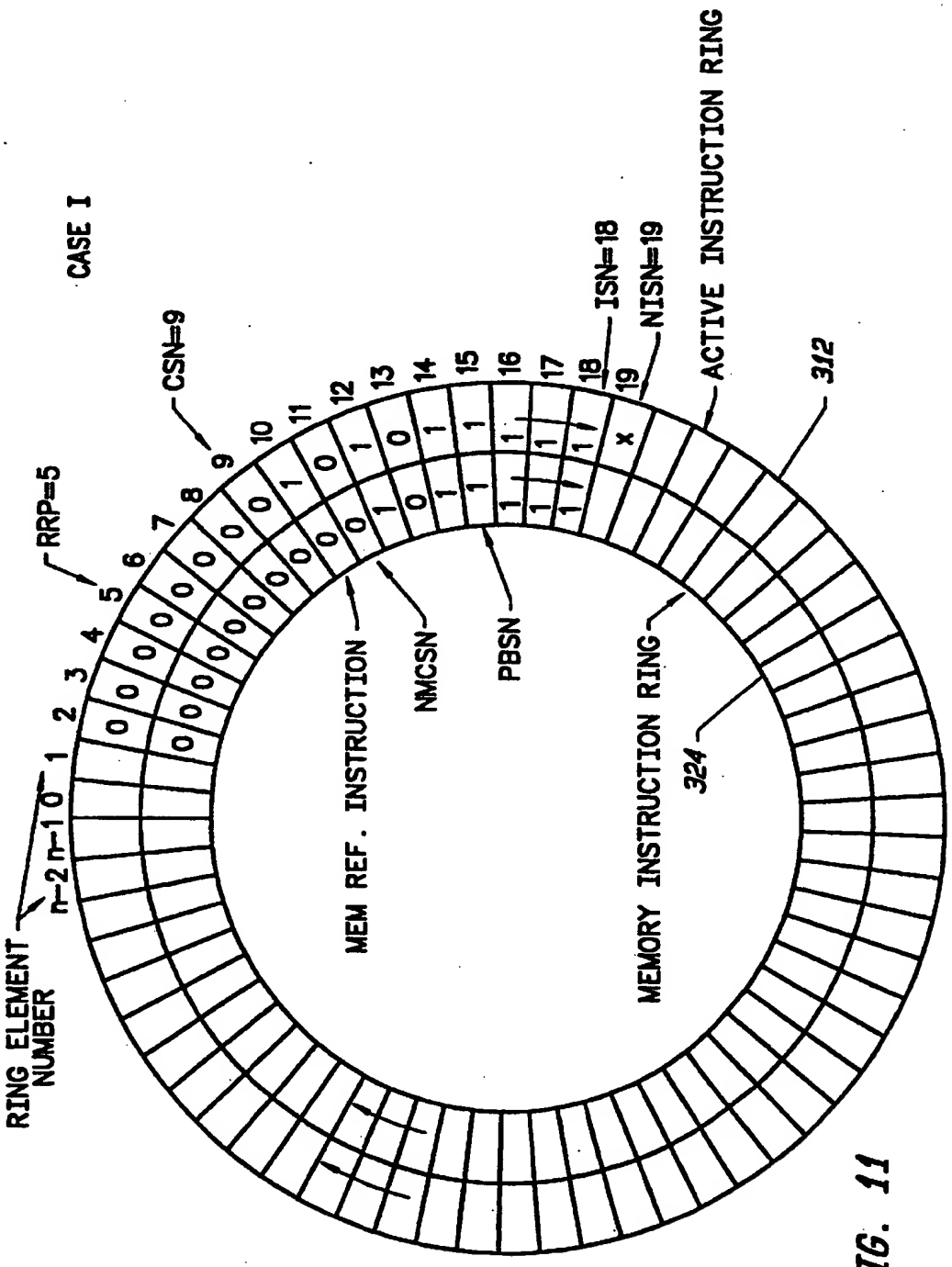
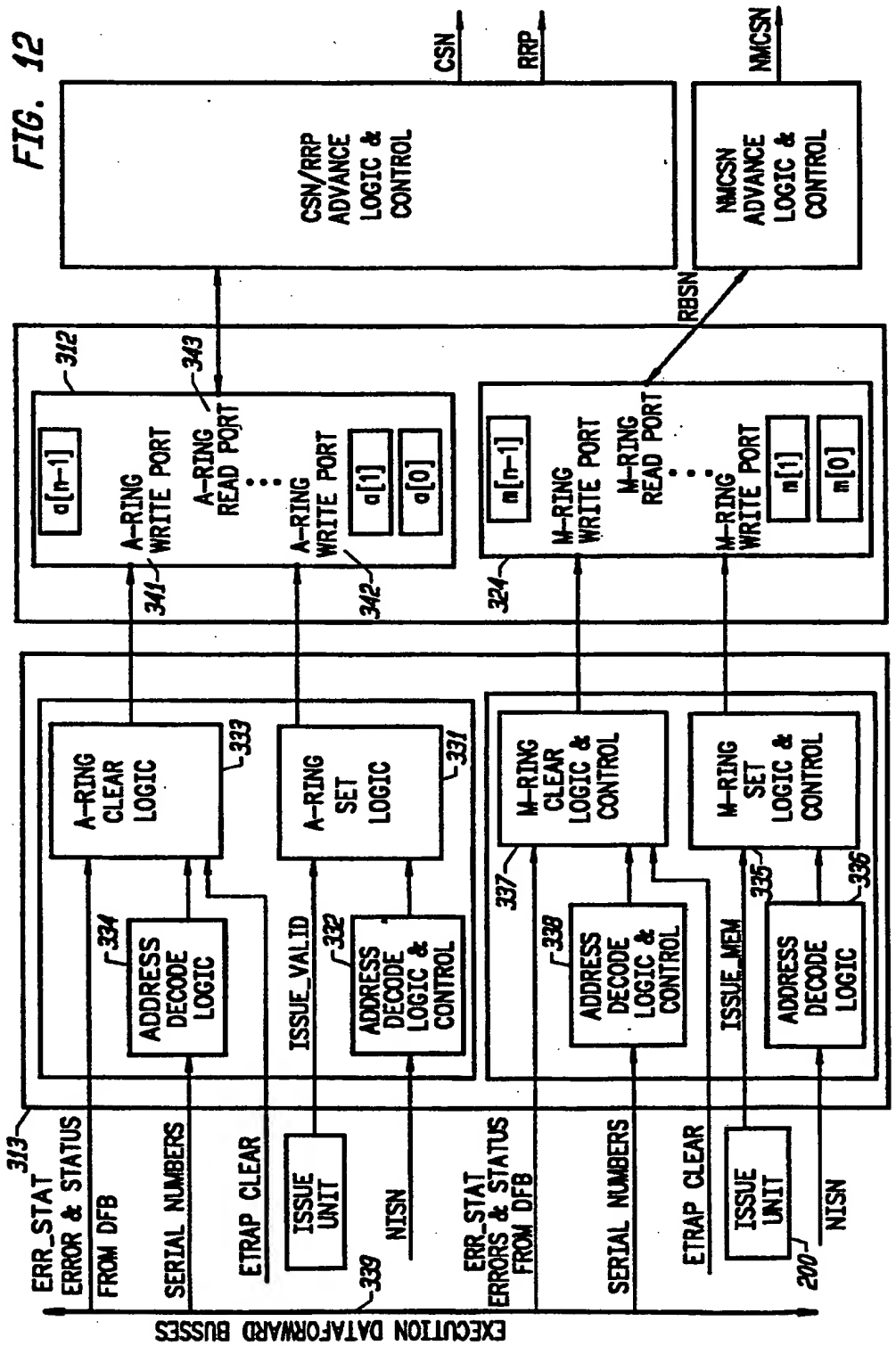

CASE I
RRP=5
CSN=9
ISN=18
NISN=19
ACTIVE INSTRUCTION RING
312
MEM REF. INSTRUCTION
NMCSN
PBSN
MEMORY INSTRUCTION RING
324
RING ELEMENT NUMBER
n-2 n-1 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

FIG. 11

	Document ID	U	Title	Current OR
1	JP 20002 42647 A	☐	METHOD AND SYSTEM FOR RETRIEVING RELATED INFORMATION	
2	JP 08030 767 A	☒	ARITHMETIC UNIT	
3	JP 04030 272 A	☒	GENERATING METHOD FOR SOLID AND VARIABLE PICTURE ELEMENT FORMING SHEET	
4	JP 03245 225 A	☒	FLOATING DECIMAL-POINT ADDITION/SUBTRACTION DEVICE	
5	JP 02255 378 A	☒	OPTICAL RECORDING MEDIUM	
6	JP 59084 314 A	☒	DEVICE FOR REPRODUCING INFORMATION RECORDING DISK	
7	WO 30656 64 A1	☒	A NETWORKING ELEMENT ADAPTED TO RECEIVE AND OUTPUT ALSO PREAMBLES OF DATA PACKETS OR FRAMES	
8	WO 30472 13 A1	☒	RADIO COMMUNICATION SYSTEM AND METHOD FOR THE OPERATION THEREOF	
9	EP 11894 10 A2	☒	Processing of data packets within a network cluster	
10	EP 10764 40 A1	☒	Method for transferring data over a packet switching network and a gateway	
11	WO 92151 50 A1	☒	SIGNAL PROCESSING APPARATUS AND METHOD	
12	WO 85007 14 A1	☒	SYSTEM FOR THE CORRECTION OF ERRORS OF DIGITAL SIGNALS CODED IN REED-SOLOMON CODE	
13	WO 20030 56766 A	☒	Scheduling packets in data network by adjusting queue sizes according to assigned weights, link bandwidth and per-hop maximum delay	
14	EP 13220 81 A	☒	Reassembling method for packets from traffic flows in network element, each packet having at least one data part, queuing each of at least one data part of packets of the traffic flows in single reassembly queue in sorted order	
15	DE 29719 815 U	☒	Head cleaning element for chip-card reader arrangement - has cleaning wipe with material for receiving debris particles arranged in area of chip, whereby material is covered with cleaning compound for magnetic heads	
16	EP 46402 5 B	☒	Data capture device for TV - extracts digital data from composite video signal and allows selective string retrieval display information on screen	
17	EP 41949 9 B	☒	High-speed vector tailgating in computers with vector registers - has element-by-element writing simultaneously with reading but lagging by one element to avoid overwriting	
18	US 46384 96 A	☒	Transmitting and receiving system for digital data transfer - forming data into composite signal with number of different signal and timing elements before transmission	
19	EP 17304 0 A	☒	Vector processing system - has pipeline unit including stage comparing exponents of vectors from two registers and effecting digit alignment	
20	DE 34856 35 G	☒	High-speed digital data processor system for vectors - uses two CPUS connected by ports to access paths of central memory, and shared registers connected to internal information paths of CPU	
21	DE 26143 62 A	☐	Composite output signal generating device - produces signal in dependence on digital signal with two parts using series of switching elements	

FIG. 12


CSN
RRP
NMCSN
CSN/RRP ADVANCE LOGIC & CONTROL
NMCSN ADVANCE LOGIC & CONTROL
RBSN
312
343
a[n-1]
A-RING WRITE PORT
A-RING READ PORT
A-RING WRITE PORT
a[1]
a[0]
341
342
m[n-1]
M-RING WRITE PORT
M-RING READ PORT
M-RING WRITE PORT
m[1]
m[0]
324
A-RING CLEAR LOGIC
333
A-RING SET LOGIC
331
M-RING CLEAR LOGIC & CONTROL
M-RING SET LOGIC & CONTROL
334
ADDRESS DECODE LOGIC
ISSUE_VALID
332
ADDRESS DECODE LOGIC & CONTROL
337
338
ADDRESS DECODE LOGIC & CONTROL
ISSUE_MEM
335
336
ADDRESS DECODE LOGIC
313
ERR_STAT ERROR & STATUS FROM DFB
SERIAL NUMBERS
ETRAP CLEAR
ISSUE UNIT
NISN
339
ERR_STAT ERRORS & STATUS FROM DFB
SERIAL NUMBERS
ETRAP CLEAR
ISSUE UNIT
NISN
200
EXECUTION DATAFORWARD BUSSES